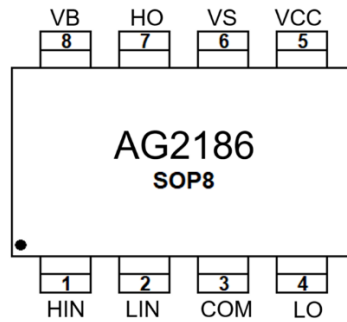






SOP8, M8

Top View

PIN#	Symbol	Function
1	HIN	High side signal input
2	LIN	Low side signal input
3	COM	ground
4	LO	Low side output
5	VCC	Power supply
6	VS	High side floating ground
7	HO	Hight side output
8	VB	High side floating supply

**ABSOLUTE MAXIMUM RATINGS** $T_A = 25^{\circ}\text{C}$, unless otherwise specified.

V_B , High-Side Floating Supply Voltage		-0.3V ~ 725V
V_S , High-Side Floating Reference Voltage		$V_B - 25\text{V} \sim V_B + 0.3\text{V}$
V_{HO} , High-Side Output Voltage		$V_S - 0.3\text{V} \sim V_B + 0.3\text{V}$
V_{CC} , Low-Side Supply Voltage		-0.3V ~ 25V
V_{LO} , Low-Side Output Voltage		-0.3V ~ $V_{CC} + 0.3\text{V}$
V_{IN} , Logic Input Voltage (HIN,LIN)		-0.3V ~ $V_{CC} + 0.3\text{V}$
P_D , Power dissipation		0.625W
ESD Discharge	Human Body Model (HBM)	1.5KV
	Machine Model (MM)	500V
$R_{\theta JA}$, Package dissipation rating	SOP8	200°C/W
T_{STG} , Storage Temperature Range		-55°C ~ +150°C
T_L , Lead Temperature (Soldering, 10 seconds)		300°C

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Conditions	Min.	Max.	Unit
High-Side Floating Supply Voltage	V_B	-	$V_S + 10$	$V_S + 20$	V
High-Side Floating Reference Voltage	V_S		-9	700	
High-Side Output Voltage	V_{HO}		V_S	V_B	
Low-Side Output Voltage	V_{LO}		0	V_{CC}	
Low-Side Supply Voltage	V_{CC}		10	20	
Logic Input Voltage (HIN,LIN)	V_{IN}	-	0	V_{CC}	
Environment Temperature	T_A	-	-40	125	°C

**ELECTRICAL CHARACTERISTICS** $V_{CC}=V_B=15V$, $C_L=1nF$, $T_A=25^{\circ}C$, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamics Characteristics						
Turn-On Propagation Delay	t _{ON}	V _S =0	130	-	250	ns
Turn-Off Propagation Delay	t _{OFF}	V _S =0, or 700V	130	-	250	
Turn-On Rise Time	t _R	V _S =0	15	-	20	
Turn-Off Fall Time	t _F		10	-	15	
Propagation Delay Matching (t _{ON} , t _{OFF})	MT		-	-	50	
Static Characteristics						
V _{CC} UVLO Rising Threshold	V _{CCUV+}	-	8	8.9	9.8	
V _{CC} UVLO Falling Threshold	V _{CCUV-}	-	7.4	8.2	9.0	
V _{CC} UVLO Hysteresis	V _{CCUVHYS}		-	0.7	-	
V _{BS} UVLO Rising Threshold	V _{BSUV+}		8	8.9	9.8	
V _{BS} UVLO Falling Threshold	V _{BSUV-}		7.4	8.2	9.0	
V _{BS} UVLO Hysteresis	V _{BSUVHYS}		-	0.7	-	
High-Side Floating Supply Leakage Current	I _{LK}		-	-	50	
V _{BS} Quiescent Current	I _{QBS}		-	50	100	
V _{CC} Quiescent Current	I _{QCC}		-	150	240	
High-Level Input Threshold Voltage	V _{IH}		2.5	-	-	
Low-Level Input Threshold Voltage	V _{IL}		-	-	0.8	
Supply-to-Output High-Level Voltage Difference	V _{OH}		-	-	1.4	
Output Low-Level-to-Ground Voltage Difference	V _{OL}		-	-	0.1	
Logic “1” Input Bias Current	I _{IN+}		-	25	60	
Logic “0” Input Bias Current	I _{IN-}	-	-	-	2	
High-Level Output Short-Circuit Pulsed Current	I _{O+}	-	3.0	4.0		
Low-Level Output Short-Circuit Pulsed Current	I _{O-}	-	3.0	4.0		
Propagation delay matching	T _{MATCH}		-5	-	5	ns



TYPICAL PERFORMANCE CHARACTERISTICS

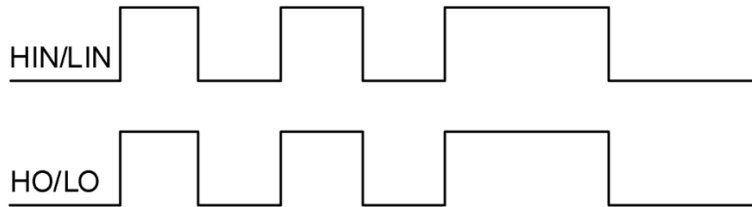


Fig 1. Input and Output Timing Waveforms

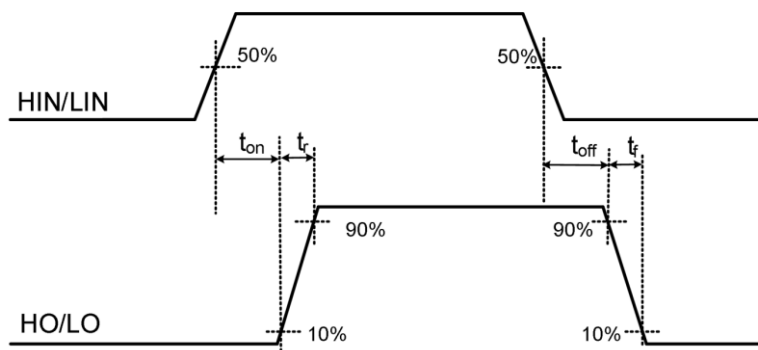


Fig 2. Propagation Delay Timing Definitions

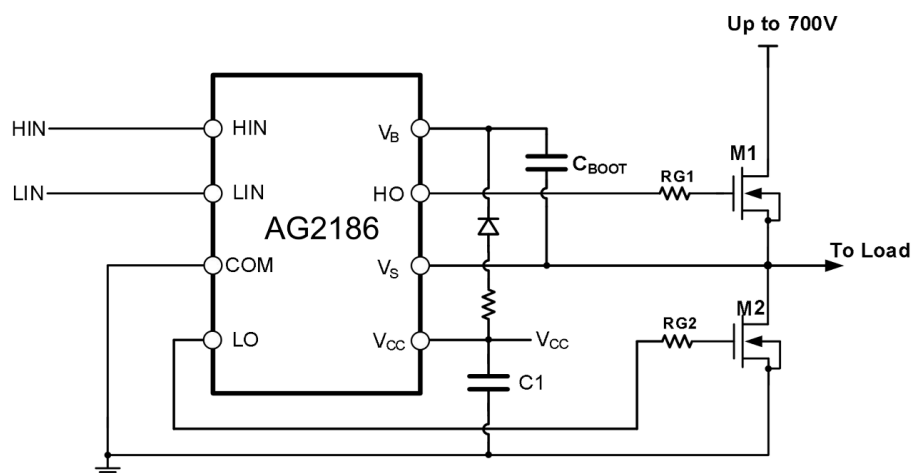
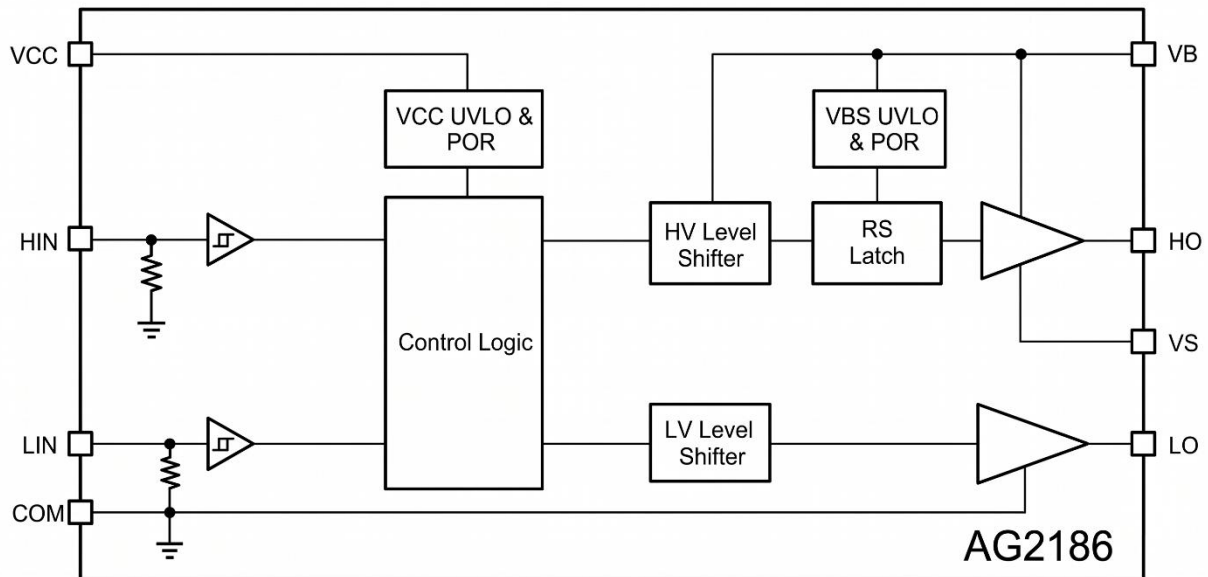


Fig 3. Typical application circuit

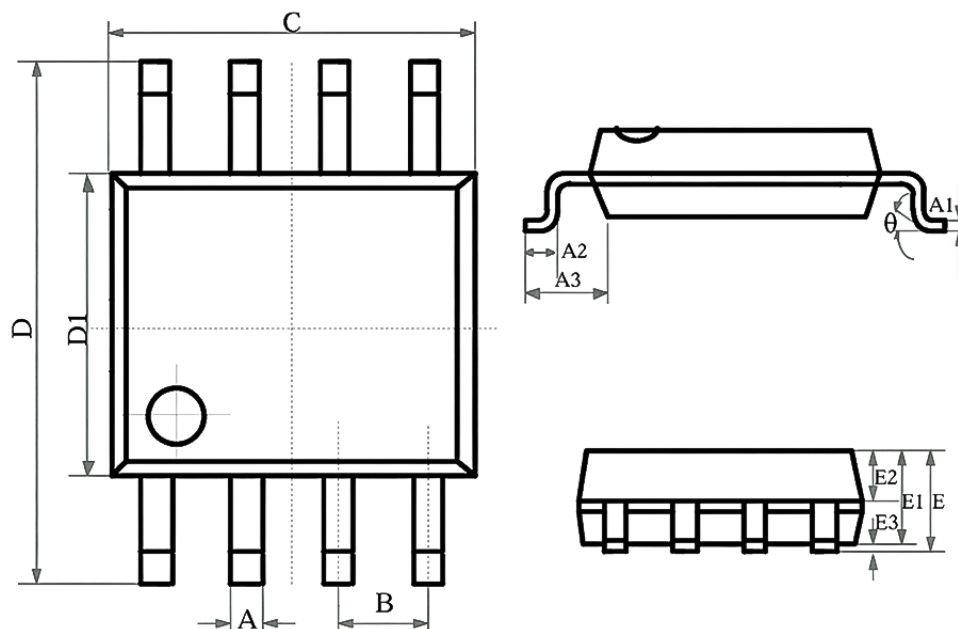
**BLOCK DIAGRAM****Layout and connection guidelines**

The AG2186 incorporates fast reacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 4A to facilitate voltage transition times. The following layout and connection guidelines are strongly recommended:

- Keep high current output and power ground paths separate from logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.
- If the inputs to a channel are not externally connected, the internal pull-down resistor indicated on block diagrams commands a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The AG2186 is compatible with many other industry standard drivers. In single input parts with enable pins, there is an internal pull-down resistor tied to GND to enable the driver by default; this should be considered in the PCB layout.
- The turn on and turn off current paths should be minimized. The Fig 3, Typical Application Circuit shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized bypass capacitor acts to contain the high peak current pulses within this driver MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

**PACKAGE INFORMATION**

Dimension in SOP8 (Unit: mm)



Symbol	Min.	Max.
A	0.39-	0.480
A1	0.210	0.280
A2	0.500	0.800
A3	1.050 BSC.	
B	1.270 BSC.	
C	4.700	5.100
D	5.800	6.200
D1	3.700	4.100
E	-	1.750
E1	1.300	1.500
E2	0.600	0.700
E3	0.100	0.225
θ	0°	8°



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