



## DESCRIPTION

The A6518D (-Q) is a low-dropout (LDO) linear regulators combine low quiescent current with excellent line and load transient response, making it well suited for battery-powered and noise-sensitive applications. The devices feature high power-supply rejection ratio (PSRR), low output noise, and fast start-up, while consuming only 45µA (typical) of quiescent current.

Fabricated using an advanced BICMOS process, the A6518D (-Q) is stable with ceramic output capacitors and achieves a typical dropout voltage of 250mV at 500mA output current. A precision voltage reference and feedback control loop provide  $\pm 0.75\%$  output voltage accuracy over the specified operating conditions.

The A6518D (-Q) is available in SOT-25, DFN6 (2x2), and DFN8 (3x3) packages.

## ORDERING INFORMATION

- Post DC-DC Converter Ripple Filtering
- IP Network Cameras
- Macro Base Stations
- Thermostats

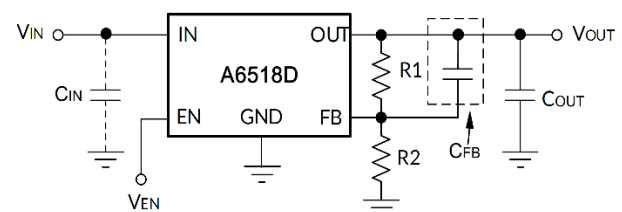
## ORDERING INFORMATION

| Package Type                    | Part Number                                           |              |
|---------------------------------|-------------------------------------------------------|--------------|
| SOT-25<br>SPQ: 3,000pcs/Reel    | E5                                                    | A6518DE5VR   |
|                                 |                                                       | A6518DE5VR-Q |
| DFN6(2x2)<br>SPQ:3,000pcs/Reel  | J6                                                    | A6518DJ6VR   |
|                                 |                                                       | A6518DJ6VR-Q |
| DFN8(3x3)<br>SPQ: 5,000pcs/Reel | J8                                                    | A6518DJ8VR   |
|                                 |                                                       | A6518DJ8VR-Q |
| Note                            | R: Tape & Reel<br>V: Halogen free Package<br>Q: AEC-Q |              |
| AiT provides all RoHS products  |                                                       |              |

## FEATURES

- Qualified for Automotive Applications
- Input Voltage Range: 2.7 V to 6.5 V
- Output Voltage Options: 1.2 V to 6.0V
- Output Current: Up to 500 mA
- Very Low Dropout Voltage: 250 mV at 500 mA ( $V_{OUT} = 3.3$  V)
- Low Quiescent Current: 45 µA
- High PSRR: 75 dB at 100 Hz
- Excellent Line and Load Transient Response
- Stable with a 2.2 µF Low-ESR Ceramic Output Capacitor
- Fast Start-Up Time: 45 µs (typical)
- High Output Voltage Accuracy:  $\pm 0.75\%$
- Operation temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .
- Available in SOT-25, DFN6 (2x2), and DFN8 (3x3) Packages

## TYPICAL APPLICATION

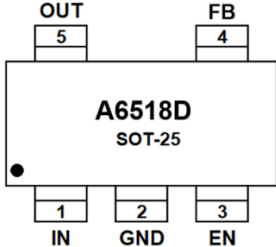
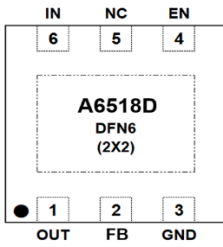
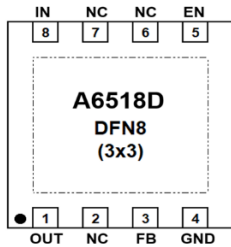


$C_{IN}$  : To improve source voltage noise and PSRR.

$C_{FB}$  : Optional feed-forward capacitor, it improves transient noise

$C_{OUT}$  : A  $\geq 2.2\mu\text{F}$  ceramic capacitor.

**PIN DESCRIPTION**

|  <p><b>A6518D</b><br/>SOT-25</p> <p>SOT-25, E5<br/>Top View</p> |             |             |  <p><b>A6518D</b><br/>DFN6<br/>(2X2)</p> <p>DFN6(2x2), J6<br/>Top View</p> |     |                                                                                                                                                                             |  <p><b>A6518D</b><br/>DFN8<br/>(3x3)</p> <p>DFN8(3x3), J8<br/>Top View</p> |  |  |
|--------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|
| PIN#                                                                                                                                             |             |             | Symbol                                                                                                                                                      | I/O | Function                                                                                                                                                                    |                                                                                                                                                               |  |  |
| SOT-25                                                                                                                                           | DFN6(2x2)   | DFN8(3x3)   |                                                                                                                                                             |     |                                                                                                                                                                             |                                                                                                                                                               |  |  |
| 1                                                                                                                                                | 6           | 8           | IN                                                                                                                                                          | I   | Input supply.                                                                                                                                                               |                                                                                                                                                               |  |  |
| 2                                                                                                                                                | 3           | 4           | GND                                                                                                                                                         | G   | Ground.                                                                                                                                                                     |                                                                                                                                                               |  |  |
| 3                                                                                                                                                | 4           | 5           | EN                                                                                                                                                          | I   | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used. |                                                                                                                                                               |  |  |
| 4                                                                                                                                                | 2           | 3           | FB                                                                                                                                                          | -   | This pin is the input to the control-loop error amplifier and is used to program the device output voltage.                                                                 |                                                                                                                                                               |  |  |
| 5                                                                                                                                                | 1           | 1           | OUT                                                                                                                                                         | O   | This pin is the output of the regulator. A small 2.2μF ceramic capacitor is required from this pin to ground to assure stability                                            |                                                                                                                                                               |  |  |
| -                                                                                                                                                | 5           | 2, 6, 7     | NC                                                                                                                                                          | -   | Not internally connected.                                                                                                                                                   |                                                                                                                                                               |  |  |
| -                                                                                                                                                | Thermal Pad | Thermal Pad | -                                                                                                                                                           | -   | The pad must be tied to the GND pin.                                                                                                                                        |                                                                                                                                                               |  |  |

**ABSOLUTE MAXIMUM RATINGS** $T_A = 25^{\circ}\text{C}$ , unless otherwise specified. <sup>(2)</sup>

|                                                          |                                                         |                              |
|----------------------------------------------------------|---------------------------------------------------------|------------------------------|
| $V_{IN}$ , Input voltage                                 |                                                         | -0.3V ~ +7V                  |
| $V_{EN}$ , Enable input voltage                          |                                                         | -0.3V ~ $V_{IN}+0.3\text{V}$ |
| $V_{FB}$ , Input voltage                                 |                                                         | -0.3V ~ +1.6V                |
| $V_{OUT}$ , Output voltage                               |                                                         | 1.2V ~ $V_{IN}+0.3\text{V}$  |
| $I_{OUT}$ , Current                                      |                                                         | Internally limited           |
| $\theta_{JA}$ , Package thermal impedance <sup>(3)</sup> | SOT-25                                                  | 200°C/W                      |
|                                                          | DFN8(3x3)                                               | 60°C/W                       |
|                                                          | DFN6(2x2)                                               | 82°C/W                       |
| $T_J$ , Junction Temperature <sup>(4)</sup>              |                                                         | -40°C ~ +150°C               |
| $T_{STG}$ , Storage Temperature Range                    |                                                         | -55°C ~ +150°C               |
| $V_{(ESD)}$ Electrostatic discharge                      | Human-Body Model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2KV                         |
|                                                          | Charged-Device Model (CDM), per AEC Q100-011            | ±1KV                         |
|                                                          | Latch-Up (LU), per AEC Q100-004                         | ±200mA                       |
| $T_L$ , Lead Temperature (Soldering, 10 seconds)         |                                                         | -55°C ~ +150°C               |

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) All voltages are with respect to the GND pin.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PCB.

**RECOMMENDED OPERATING CONDITIONS** $T_A = 25^{\circ}\text{C}$  (Room Temperature), unless otherwise specified.

| Parameter                              | Conditions | Min      | Typ | Max | Unit |
|----------------------------------------|------------|----------|-----|-----|------|
| $V_{IN}$ , Supply Voltage              |            | 2.7      | -   | 6.5 | V    |
| $V_{OUT}$ , Output Voltage             |            | $V_{FB}$ |     | 6.0 | V    |
| $T_A$ , Ambient Operating Temperature  |            | -40      | -   | 125 | °C   |
| $T_J$ , Operating Junction Temperature |            | -40      |     | 150 | °C   |
| Output Current                         |            | 0        |     | 500 | mA   |

**ELECTRICAL CHARACTERISTICS**

Over operating temperature range ( $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUTnom} + 0.5\text{ V}$  or  $2.7\text{ V}$  (whichever is greater),  $I_{OUT}=1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ , and  $T_A = 25^{\circ}\text{C}$ ,  $V_{OUT}=3.3\text{V}$  unless otherwise specified

| Parameter                                      | Symbol                   | Conditions                                                                      | Min.                                                  | Typ.  | Max.                | Unit |                   |
|------------------------------------------------|--------------------------|---------------------------------------------------------------------------------|-------------------------------------------------------|-------|---------------------|------|-------------------|
| POWER SUPPLY AND CURRENTS                      |                          |                                                                                 |                                                       |       |                     |      |                   |
| Input Voltage <sup>(1)</sup>                   | V <sub>IN</sub>          | -                                                                               | 2.70                                                  | -     | 6.50                | V    |                   |
| Under Voltage Lockout                          | UVLO                     | V <sub>IN</sub> rising, T <sub>J</sub> = -40°C ~125°C                           | 2.25                                                  | 2.4-5 | 2.65                | V    |                   |
| Hysteresis                                     | V <sub>HYS</sub>         | V <sub>IN</sub> falling                                                         | -                                                     | 60    | -                   | mV   |                   |
| Quiescent Current                              | I <sub>Q</sub>           | I <sub>OUT</sub> = 0mA, T <sub>J</sub> = 25°C                                   | -                                                     | 45    | 70                  | μA   |                   |
|                                                |                          | I <sub>OUT</sub> = 0mA, T <sub>J</sub> = -40°C ~125°C                           | -                                                     | -     | 80                  |      |                   |
| Ground Pin Current                             | I <sub>GND</sub>         | 10mA ≤ I <sub>OUT</sub> ≤ 500mA, T <sub>J</sub> = 25°C                          | -                                                     | 70    | 120                 | μA   |                   |
|                                                |                          | 10mA ≤ I <sub>OUT</sub> ≤ 500mA,<br>T <sub>J</sub> = -40°C ~125°C               | -                                                     | -     | 350                 |      |                   |
| Shutdown Current                               | I <sub>SD</sub>          | V <sub>EN</sub> = 0V, T <sub>J</sub> = 25°C                                     | -                                                     | 0.10  | 1                   | μA   |                   |
|                                                |                          | V <sub>EN</sub> = 0V, T <sub>J</sub> = -40°C ~125°C                             | -                                                     | -     | 15                  |      |                   |
| OUTPUT VOLTAGE                                 |                          |                                                                                 |                                                       |       |                     |      |                   |
| Output Voltage Range                           | V <sub>OUT</sub>         | Adjustable Voltage Output                                                       | V <sub>FB</sub>                                       | -     | 6.0                 | V    |                   |
| Feedback Voltage                               | V <sub>FB</sub>          |                                                                                 | 1.191                                                 | 1.2   | 1.209               |      |                   |
| Feedback Pin Current                           | I <sub>FB</sub>          |                                                                                 |                                                       | 0.01  | 0.1                 | μA   |                   |
| DC Output Accuracy <sup>(1)</sup>              | ΔV <sub>OUT</sub>        | T <sub>J</sub> = 25°C                                                           | -0.75                                                 | -     | 0.75                | %    |                   |
|                                                |                          | T <sub>J</sub> = -40°C ~125°C                                                   | -1.50                                                 | -     | 1.50                |      |                   |
| Line Regulation <sup>(1)</sup>                 | ΔV <sub>OUT(ΔVIN)</sub>  | V <sub>OUTnom</sub> + 0.5V ≤ V <sub>IN</sub> ≤ 6.5V                             | -                                                     | 0.02  | 0.06                | %/V  |                   |
| Load Regulation                                | ΔV <sub>OUT(ΔIOUT)</sub> | 500μA ≤ I <sub>OUT</sub> ≤ 500mA                                                | -                                                     | 0.002 | 0.006               | V/mA |                   |
| DROPOUT VOLTAGE                                |                          |                                                                                 |                                                       |       |                     |      |                   |
| Dropout Voltage <sup>(2)</sup>                 | V <sub>DO</sub>          | I <sub>OUT</sub> =<br>500mA                                                     | V <sub>OUT</sub> =3.3V, T <sub>J</sub> = 25°C         | -     | 250                 | 300  | mV                |
|                                                |                          |                                                                                 | V <sub>OUT</sub> =3.3V, T <sub>J</sub> = -40°C ~125°C | -     | -                   | 400  |                   |
| POWER SUPPLY REJECTION RATIO AND NOISE         |                          |                                                                                 |                                                       |       |                     |      |                   |
| Power Supply<br>Rejection Ratio <sup>(3)</sup> | PSRR                     | V <sub>IN</sub> = 3.8V,<br>V <sub>OUT</sub> = 3.3V,<br>I <sub>OUT</sub> = 100mA | f = 100Hz                                             | -     | 75                  | -    | dB                |
|                                                |                          |                                                                                 | f = 1kHz                                              | -     | 64                  | -    |                   |
|                                                |                          |                                                                                 | f = 10kHz                                             | -     | 43                  | -    |                   |
|                                                |                          |                                                                                 | f = 100kHz                                            | -     | 23                  | -    |                   |
| Output Noise Voltage <sup>(3)</sup>            | V <sub>N</sub>           | BW = 10 Hz to 100<br>kHz, V <sub>OUT</sub> = 3.3 V                              |                                                       |       | 45×V <sub>OUT</sub> |      | μV <sub>RMS</sub> |



| ENABLE AND STARTUP TIME         |           |                                                                                                        |     |      |      |                    |
|---------------------------------|-----------|--------------------------------------------------------------------------------------------------------|-----|------|------|--------------------|
| Enable High(enabled)            | $V_{IH}$  | EN rising, $T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$                                        | 1.2 | -    | -    | V                  |
| Enable Low(shutdown)            | $V_{IL}$  | EN falling, $T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$                                       | -   | -    | 0.4  | V                  |
| Enable Pin Current,<br>Enabled  | $I_{EN}$  | $V_{EN} = V_{IN} = 6.5\text{V}$ , $T_J = 25^{\circ}\text{C}$                                           | -   | 0.10 | 1.5  | $\mu\text{A}$      |
|                                 |           | $V_{EN} = V_{IN} = 6.5\text{V}$ , $T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$                 | -   | -    | 2    |                    |
| Startup Time <sup>(3)</sup>     | $t_{STR}$ |                                                                                                        | -   | 45   | -    | $\mu\text{s}$      |
| PROTECTIONS                     |           |                                                                                                        |     |      |      |                    |
| Output Current Limit            | $I_{LIM}$ | $V_{OUT} = 0.9 \times V_{OUTnom}$ ,<br>$V_{IN} = V_{OUTnom} + 0.5\text{V}$ , $V_{IN} \geq 2.7\text{V}$ | 500 | 1150 | 1600 | mA                 |
| Thermal Shutdown<br>Temperature | $T_{SD}$  | Shutdown, temperature increasing                                                                       | -   | 150  | -    | $^{\circ}\text{C}$ |
|                                 |           | Reset, temperature decreasing                                                                          | -   | 135  | -    | $^{\circ}\text{C}$ |

(1) Minimum  $V_{IN} = V_{OUT} + V_{DO}$  or 2.7V, whichever is greater.

(2)  $V_{DO}$  FT test method: test the  $V_{OUT}$  voltage at  $V_{OUTnom} + V_{DOMAX}$  with output current.

(3) Guaranteed by design and characterization, not a FT item.



## TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Line Regulation

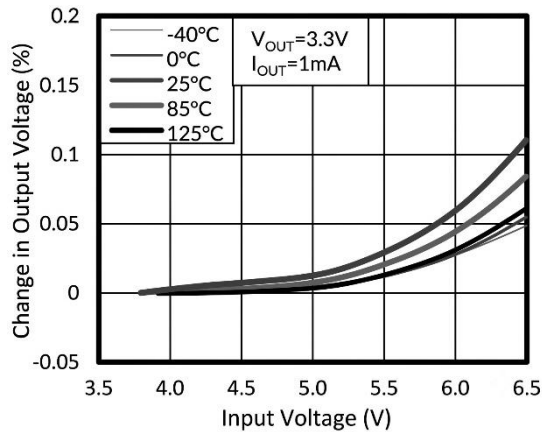


Fig 2. Line Regulation

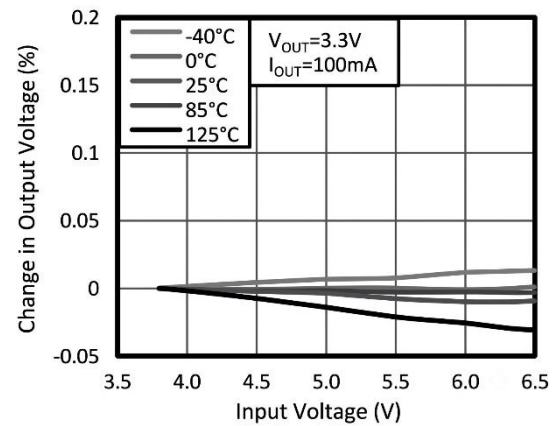


Fig 3. Output Voltage vs. Junction Temperature

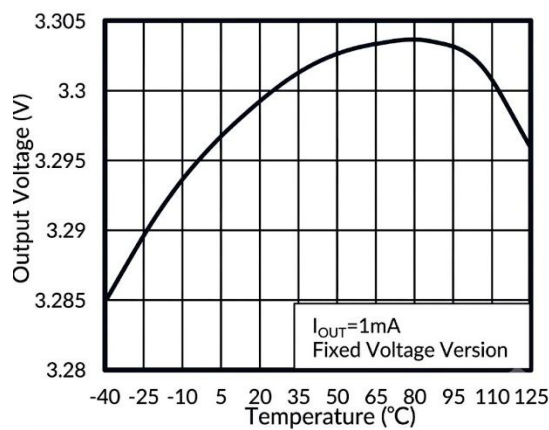


Fig 4. Feedback Voltage vs. Junction Temperature

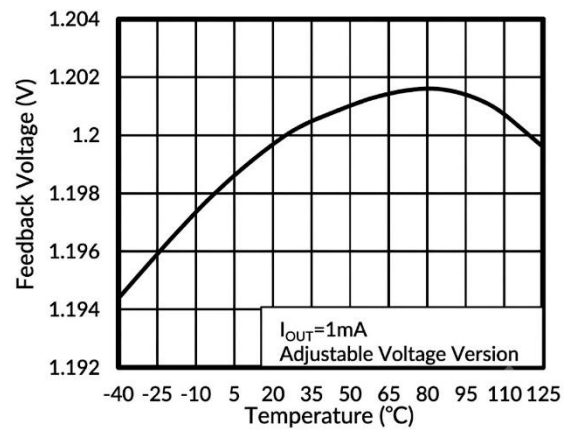


Fig 5. Feedback Pin Current vs. Junction Temperature

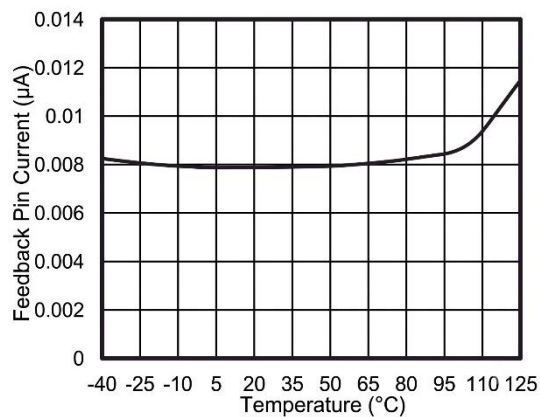


Fig 6. UVLO vs. Junction Temperature

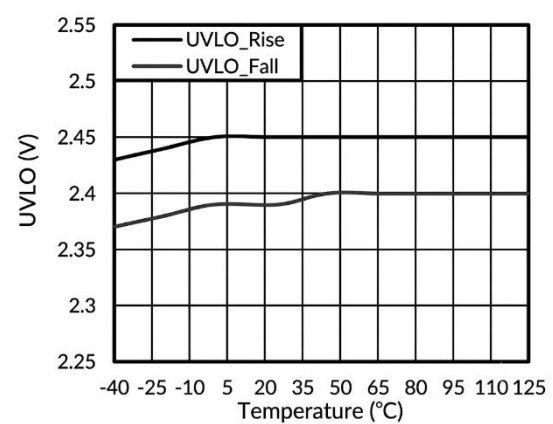




Fig 7. Quiescent Current vs Input Voltage

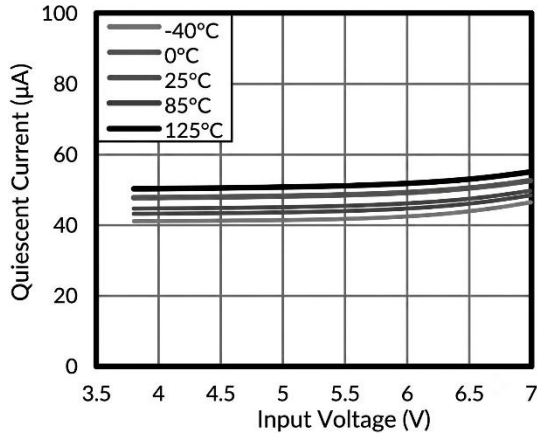


Fig 8. Quiescent Current vs Temperature

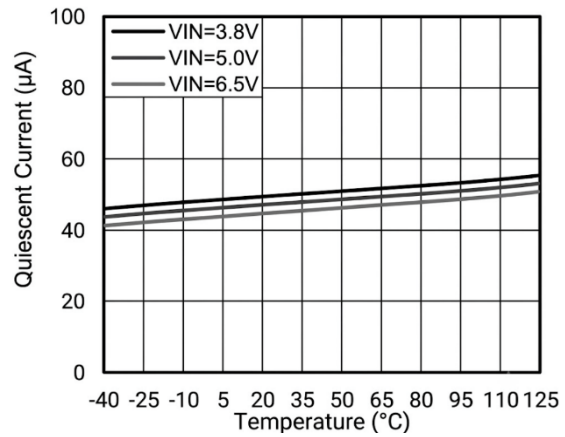


Fig 9. Ground Pin Current vs Output Current

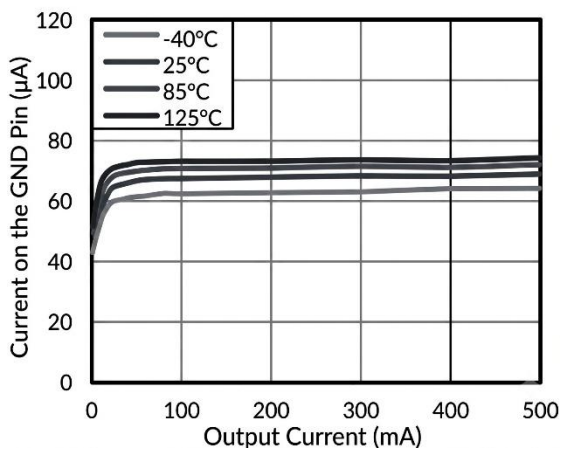


Fig 10. Supply Current vs Input Voltage

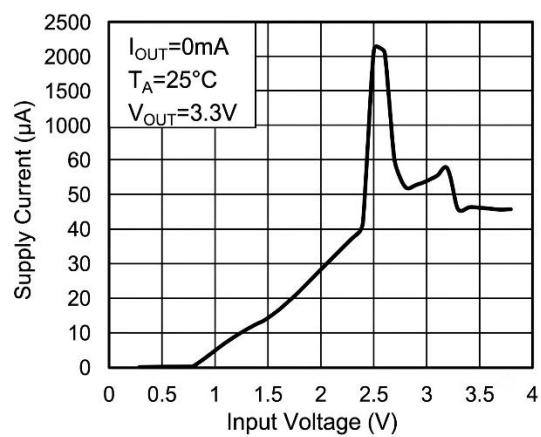


Fig 11. Shutdown Current vs Temperature

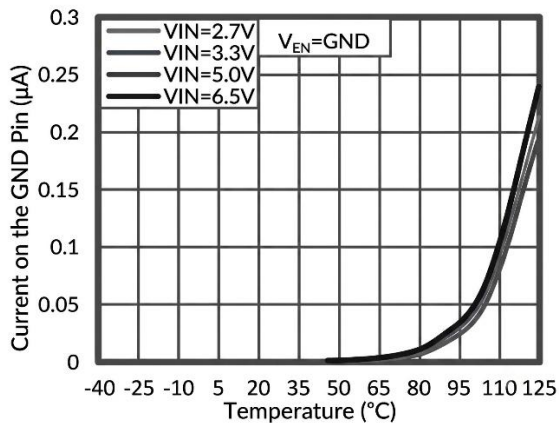


Fig 12. Load Regulation

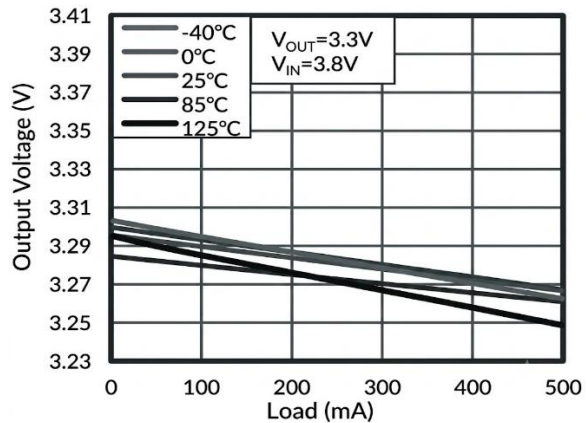




Fig 13. Output Current Limit vs. Temperature

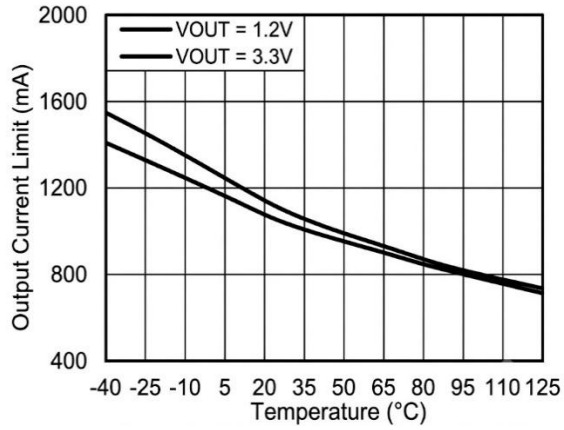


Fig 14. Line Transient Response

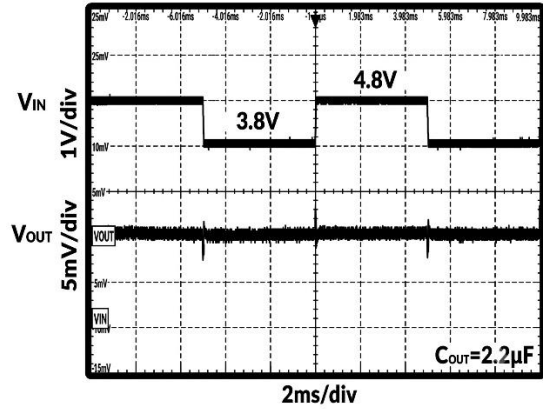


Fig 15. Load Transient Response

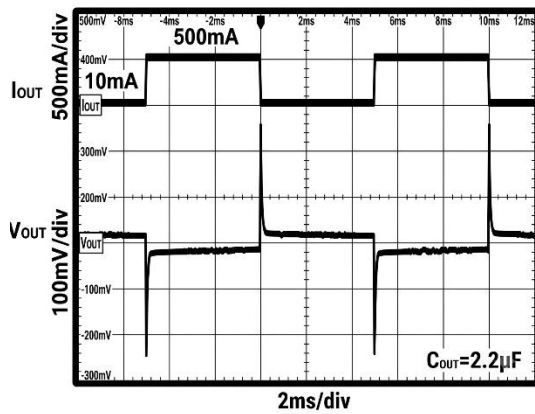


Fig 16. Load Transient Response

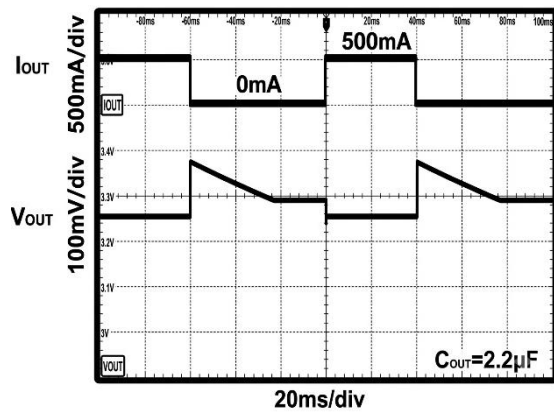


Fig 17. Power On

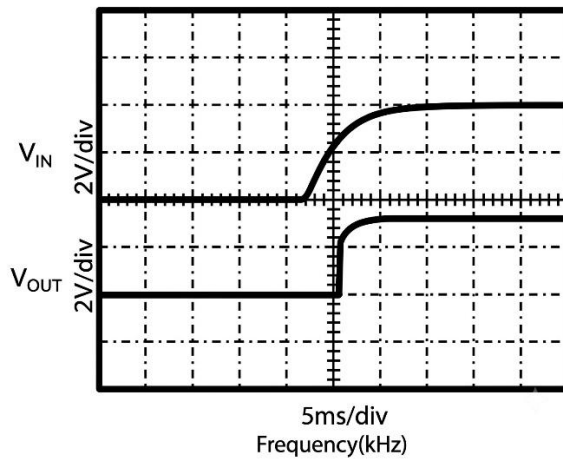


Fig 18. Power Off

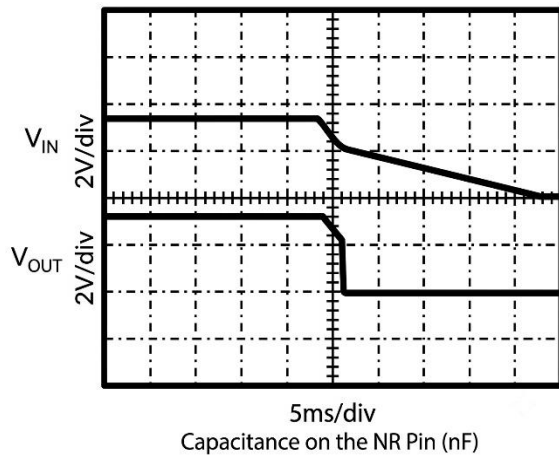




Fig 19. Enable Threshold vs. Input Voltage

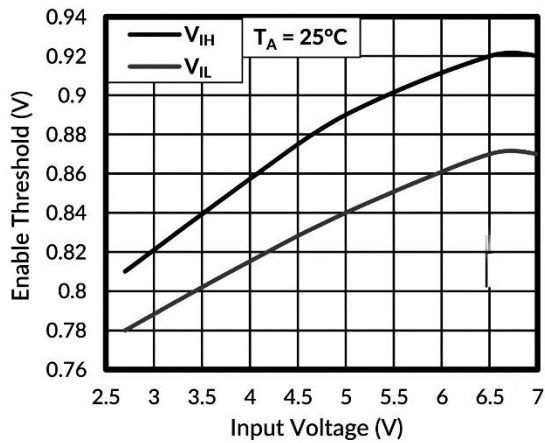


Fig 20. Enable Threshold vs. Junction Temperature

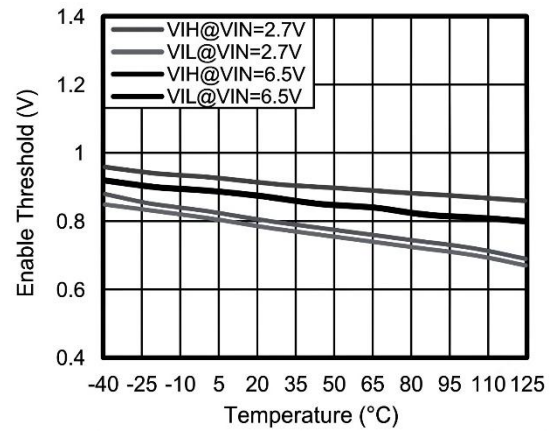


Fig 21. Dropout Voltage vs. Output Current

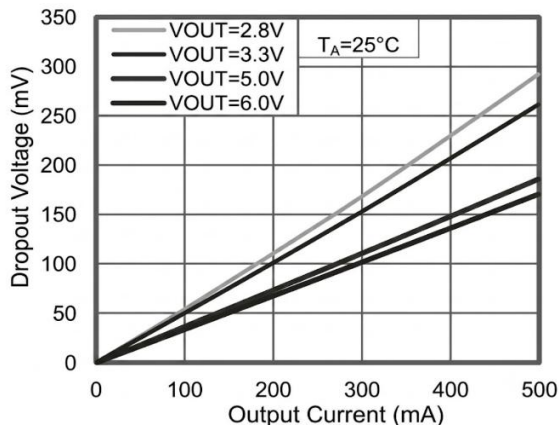


Fig 22. Dropout Voltage vs. Output Current

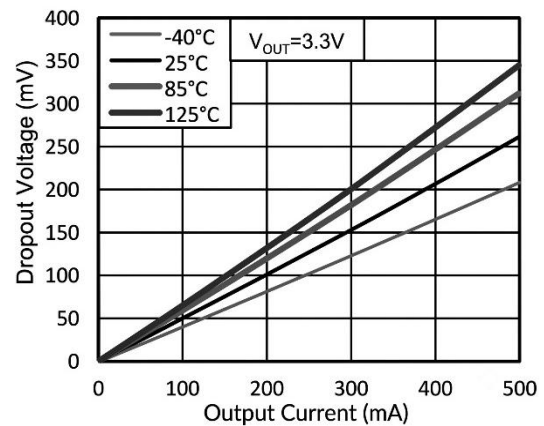


Fig 23. Power Supply Rejection Ratio vs. Frequency

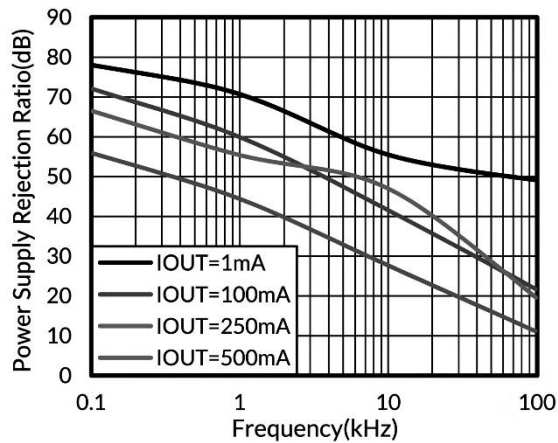


Fig 24. RMS Noise vs. C<sub>NR</sub>

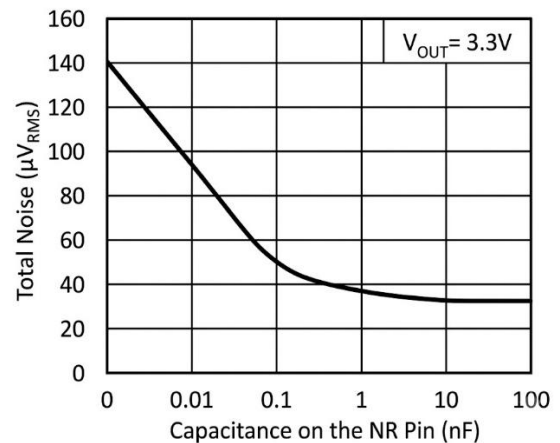




Fig 25. Turn-Off Response Using EN

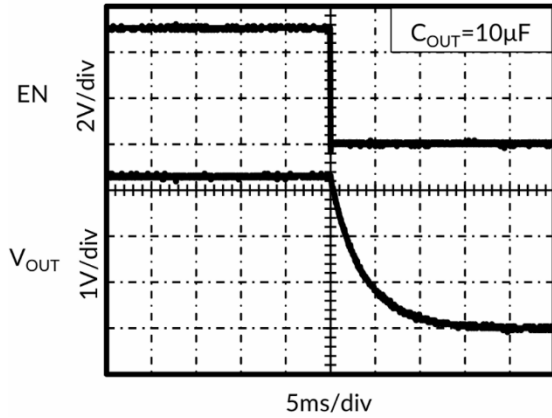


Fig 26. Turn-Off Response Using EN

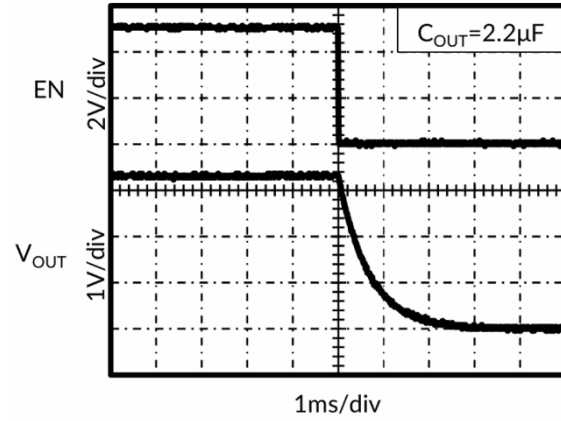


Fig 27. Turn-On Response Using EN

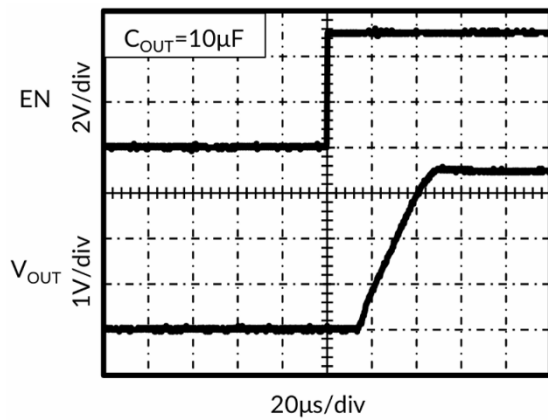
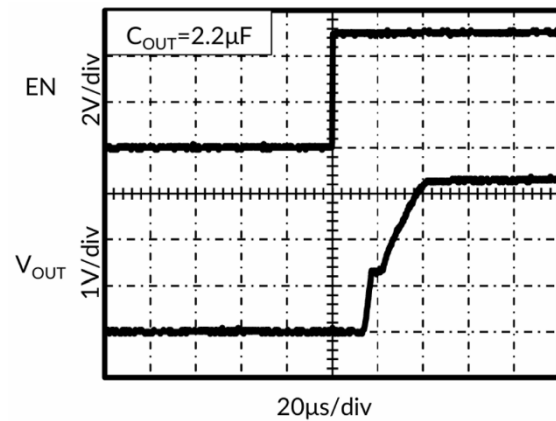


Fig 28. Turn-On Response Using EN





## FEATURE DESCRIPTION

### Internal Current-Limit

The A6518D (-Q) incorporates an internal current-limit circuit to protect the device under fault conditions. During current limiting, the output current is regulated to a fixed level that is largely independent of the output voltage. To ensure reliable operation, prolonged operation in the current-limit condition is not recommended. The A6518D (-Q) also integrates an internal body diode between the OUT and IN pins. When the voltage at OUT exceeds the voltage at IN, the body diode conducts reverse current. Since this current is not internally limited, external current-limiting or protection circuitry should be provided if prolonged reverse-voltage conditions are expected.

### Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the IN pin.

### Transient Response

As with most LDO regulators, increasing the output capacitance reduces output voltage overshoot and undershoot during load transients, but also increases the settling time. For the adjustable output, an optional feedforward capacitor ( $C_{FB}$ ) connected between the OUT and FB pins can improve loop stability and transient response. The A6518D (-Q) porates an active output pull-down circuit that is enabled when the output voltage overshoots by approximately 4.5% or more. When activated, the pull-down circuit behaves like an equivalent 350 $\Omega$  resistor connected between OUT and GND, helping to suppress overshoot and improve transient response.

### Undervoltage Lockout (UVLO)

The A6518D (-Q) incorporates an undervoltage lockout (UVLO) circuit that keeps the regulator disabled until the input voltage is sufficient to ensure proper operation of the internal circuitry.

### Disabled

The regulator is disabled under any of the following conditions:

- The input voltage is below the UVLO falling threshold or has not yet exceeded the UVLO rising threshold.
- The EN pin voltage is below the enable falling threshold or has not yet exceeded the enable rising threshold. When the regulator is disabled, the internal active pull-down circuit behaves like an equivalent 350 $\Omega$  resistor connected between OUT and GND.
- The junction temperature exceeds the thermal shutdown threshold.



## TYPICAL APPLICATION

### Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1μF to 1μF low-equivalent series resistance (ESR) capacitor close to the regulator input supply is recommended as good analog design practice. This capacitor helps suppress the effects of reactive input sources and improves transient response and ripple rejection performance.

A larger input capacitor may be required if large, fast rise-time load transients are expected or if the device is located several inches away from the power source. If the source impedance is not sufficiently low, a 0.1μF input capacitor may be required to ensure stable operation.

The A6518D (-Q) designed to be stable with standard ceramic output capacitors of 2.2μF or greater. X5R and X7R ceramic capacitors are recommended because they provide minimal variation in capacitance and ESR over temperature, ensuring reliable stability and performance.

### Adjustable Device Feedback Resistors

The A6518D (-Q) requires an external resistor divider to set the output voltage. The output voltage is determined by the feedback resistors, R1 and R2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R1 / R2)$$

To minimize the effect of the FB pin current on the output voltage accuracy, set the feedback divider current to 100× the FB pin current specified in the Electrical Characteristics table. This condition determines the maximum allowable feedback divider resistance, as shown in the following equation:

$$R1 + R2 \leq V_{OUT} / (I_{FB} \times 100)$$

### Feed-Forward Capacitor( Optional )

The A6518D (-Q), a feed-forward capacitor ( $C_{FB}$ ) can be connected between the OUT and FB pins.  $C_{FB}$  improves transient response, noise performance, and PSRR, but it is not required for regulator stability.

Recommended  $C_{FB}$  values are listed in Table 1 for reference.

| $V_{OUT}$ (V) | $C_{OUT}$ (μF)         | $R2$ (kΩ) | $C_{FB}$ (pF) |
|---------------|------------------------|-----------|---------------|
| 1.8           | 2.2 or 4.7 or 10 or 22 | 220       | 22            |
|               |                        | 100       | 47            |
|               |                        | 47        | 100           |
| 3.3           | 2.2 or 4.7 or 10 or 22 | 220       | 22            |
|               |                        | 100       | 47            |
|               |                        | 47        | 100           |
| 5             | 2.2 or 4.7 or 10 or 22 | 220       | 22            |
|               |                        | 100       | 47            |
|               |                        | 47        | 100           |

Table 1



## POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range of 2.7V to 6.5V. The input voltage must provide sufficient headroom to allow the device to maintain a regulated output voltage. The input supply should be well regulated. If the input supply is noisy, adding additional low-ESR input capacitors can help reduce output noise.

## LAYOUT

For best overall performance, place all circuit components on the same side of the PCB and as close as possible to the corresponding LDO pin connections. The ground return connections of the input capacitor, output capacitor, and LDO ground pin should be placed as close to each other as possible and connected using a wide copper area on the component side of the PCB.

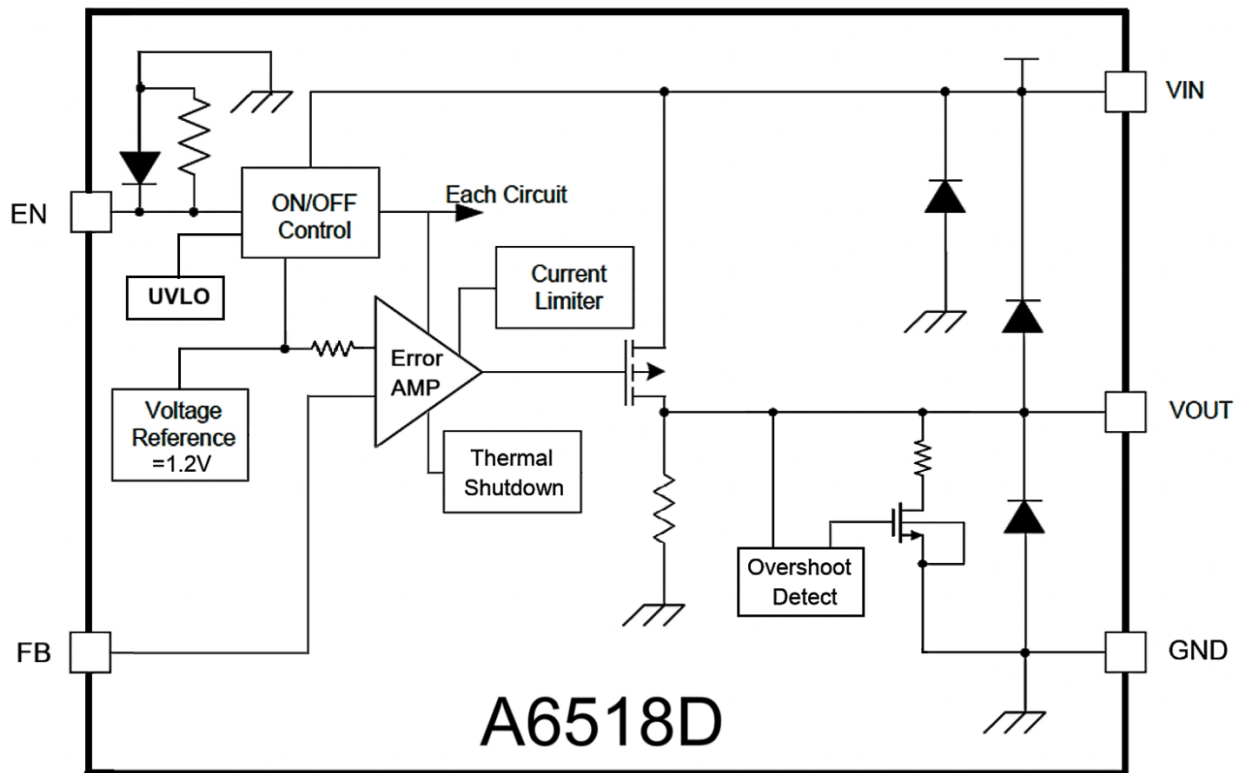
The use of vias and long traces for LDO component connections is strongly discouraged, as they introduce additional parasitic inductance and may negatively impact system performance. This grounding and layout scheme minimizes inductive parasitic, reduces load-current transient effects, minimizes noise, and improves overall circuit stability.

A ground reference plane is also recommended. The ground plane can be embedded within the PCB or placed on the bottom layer of the PCB opposite the component side. This reference plane helps maintain output voltage accuracy, provides noise shielding for the LDO, and acts as a thermal plane to distribute (or dissipate) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is required to satisfy thermal performance requirements.

To improve AC performance, such as PSRR, output noise, and transient response, it is recommended to design the PCB with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the two ground planes connected only at the LDO GND pin. In addition, the ground connection of the bypass capacitor must be connected directly to the device GND pin.



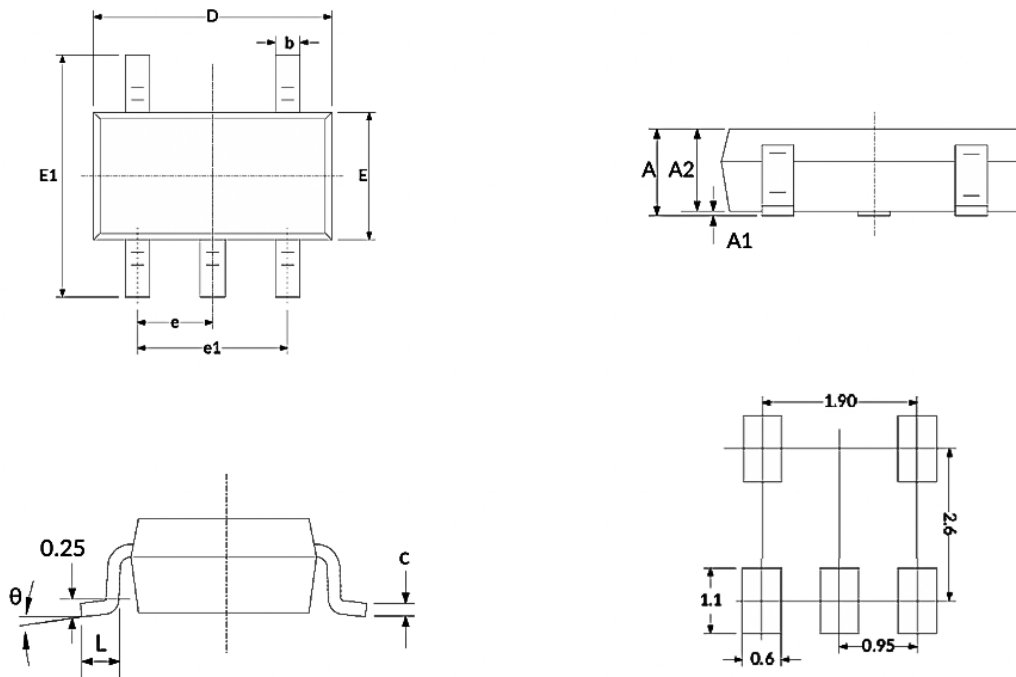
**BLOCK DIAGRAM**





## PACKAGE INFORMATION

Dimension in SOT-25 (Unit: mm)

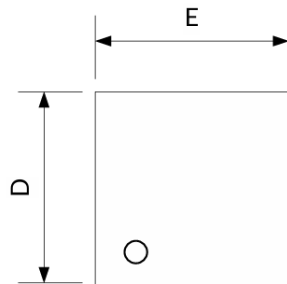


## RECOMMENDED LAND PATTERN

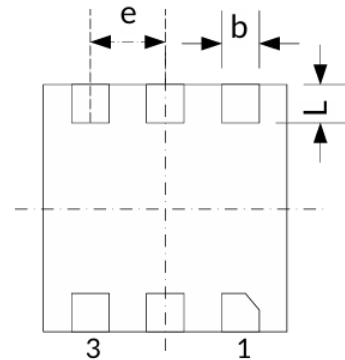
| Symbol           | Min.                      | Max.  |
|------------------|---------------------------|-------|
| A <sup>(1)</sup> | -                         | 1.250 |
| A1               | 0.000                     | 0.150 |
| A2               | 1.000                     | 1.200 |
| b                | 0.360                     | 0.55  |
| c                | 0.100                     | 0.200 |
| D <sup>(1)</sup> | 2.826                     | 3.026 |
| E <sup>(1)</sup> | 1.526                     | 1.726 |
| E1               | 2.600                     | 3.000 |
| e                | 0.950 BSC. <sup>(2)</sup> |       |
| e1               | 1.800                     | 2.000 |
| L                | 0.350                     | 0.600 |
| θ                | 0°                        | 8°    |



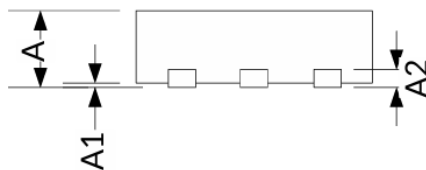
Dimension in DFN6(2x2) (Unit: mm)



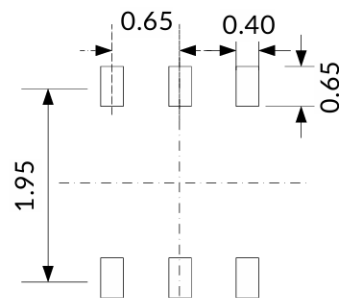
Top View



Bottom View



Side View

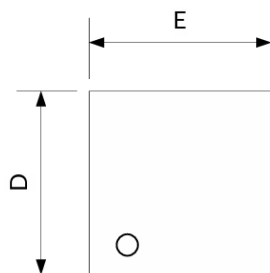


RECOMMENDED LAND PATTERN

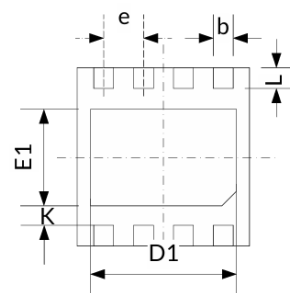
| Symbol | Min.       | Max.  |
|--------|------------|-------|
| A *    | 0.700      | 0.800 |
| A1     | 0.000      | 0.050 |
| A2     | 0.203 TYP. |       |
| b      | 0.250      | 0.350 |
| D *    | 1.900      | 2.100 |
| E *    | 1.900      | 2.100 |
| e      | 0.650 TYP. |       |
| L      | 0.250      | 0.400 |



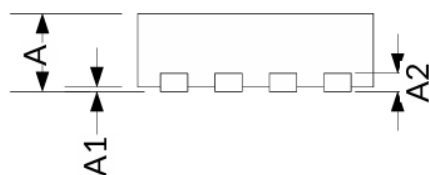
Dimension in DFN8(3x3) (Unit: mm)



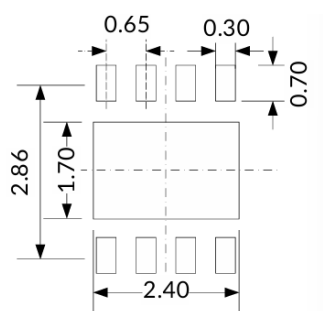
Top View



Bottom View



Side View



RECOMMENDED LAND PATTERN

| Symbol           | Min.                      | Max.  |
|------------------|---------------------------|-------|
| A <sup>(1)</sup> | 0.700                     | 0.800 |
| A1               | 0.000                     | 0.050 |
| A2               | 0.203 REF. <sup>(2)</sup> |       |
| b                | 0.200                     | 0.300 |
| D <sup>(1)</sup> | 2.900                     | 3.100 |
| D1               | 2.250                     | 2.350 |
| E <sup>(1)</sup> | 2.900                     | 3.100 |
| E1               | 1.450                     | 1.550 |
| e                | 0.650 TYP.                |       |
| L                | 0.425                     | 0.525 |
| K                | 0.200 REF.                |       |

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