DESCRIPTION

The AO4122 is a Quad CMOS operational amplifier use auto-zero techniques to simultaneously provide very low offset voltage (5μV Max) and near-zero drift over time and temperature.
This AO4122 amplifier has ultralow noise, offset and power.

This AO4122 miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 350KHz and slew rate of 0.17V/μs.

Single or dual supplies as low as +2.3V (±1.15V) and up to +5.5V (±2.75V) may be used.

The AO4122 is available in SOP14 and TSSOP14 package.

ORDERING INFORMATION

Package Type		Part Number
SOP14 SPQ:4,000pcs/Reel	M14	AO4122M14R
		AO4122M14VR
TSSOP14 SPQ:4,000pcs/Reel	TMX14	AO4122TMX14R
		AO4122TMX14VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

FEATURES

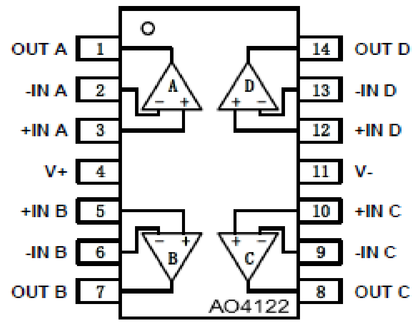
- Low Offset Voltage: 1uV(TYP.)
- Input Offset Drift: ±0.005μV/°C
- High Gain Bandwidth Product: 350KHz
- Rail-to-Rail Input and Output
- High Gain, CMRR, PSRR:130dB
- High Slew Rate: 0.17V/μs
- Low Noise: 3.2uVp-p (0.01~10Hz)
- Low Power Consumption: 60μA /op amp
- Overload Recovery Time:6us
- Low Supply Voltage: 2.3 V to 5.5 V
- No External Capacitors Required
- Extended Temperature: -40°C ~ +125°C

APPLICATION

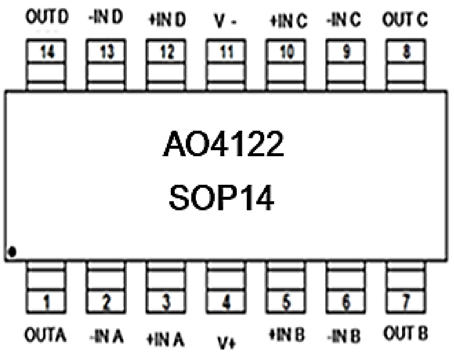
- Temperature Sensors
- Medical/Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/Inverter

TYPICAL APPLICATION

SOP14/TSSOP14

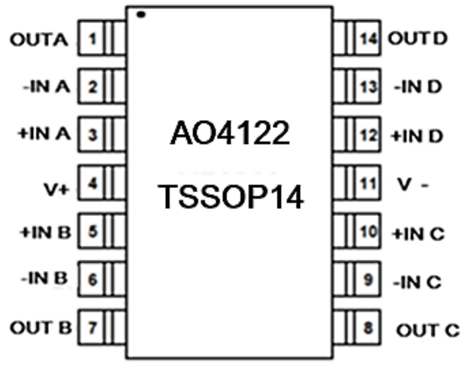


PIN DESCRIPTION



SOP14, M14

Top View



TSSOP14, TMX14

Top View

PIN#		Symbol	Function
SOP14	TSSOP14		
1	1	OUT A	Output A
2	2	-IN A	Inverting Input A
3	3	+IN A	Noninverting Input A
4	4	V-	Positive (Highest) Power Supply
5	5	+IN B	Noninverting Input B
6	6	-IN B	Inverting Input B
7	7	OUT B	Output B
8	8	OUT C	Output C
9	9	-IN C	Inverting Input C
10	10	+IN C	Noninverting Input C
11	11	V-	Negative (Lowest) Power Supply
12	12	+IN D	Noninverting Input D
13	13	-IN D	Inverting Input D
14	14	OUT D	Output D

ABSOLUTE MAXIMUM RATINGS

V_S, Supply, V_S =(V+) - (V-), Voltage		7.0V
Signal Input Pin, Voltage(1)		(V-)-0.5 to (V+)0.5V
Signal Output Pin, Voltage(2)		(V-)-0.5 to (V+)0.5V
Signal Input Pin, Current(1)		±10mA
Signal Output Pin, Current(2)		±55mA
Output Short-Circuit, Current(3)		Continuous
$θ_{JA}$, Package Thermal Impedance(4)	SOP14	105℃/W
	TSSOP14	90℃/W
T_A , Operating Range		-40℃ ~ +125℃
T_{STG}, Storage Temperature		-65℃ ~ +150℃
T_J , Junction Temperature(5)		-40℃ ~ +150℃
ESD Ratings		
$V_{(ESD)}$, Electrostatic Discharge	Human-Body Model (HBM)	±5000V
	Machine Model (MM)	±400V

*Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(1) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(2) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±55mA or less.

(3) Short-circuit to ground, one amplifier per package.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J\ (MAX)}$, $R_{θJA,}$ and T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J\ (MAX)}$ - T_A) / $R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Supply Voltage	V_S =(V+) - (V-)	Single-Supply	2.3	-	5.5	V
		Dual-Supply	±1.15		±2.75	

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM} = V_S / 2	-5	±1	5	μV
Input Offset Voltage Average Drift	V_{OS} T_C			±0.005	±0.05	μV/°C
Power-Supply Rejection Ratio	PSRR	V_S=2.3V to 5.5V, V_{CM} = 0	110	130	-	dB
Channel Separation	dc		-	0.1	-	μV/V
INPUT BIAS CURRENT						
Input Bias Current(1)(2)	I_B	V_{CM} = Vs/2	-	±10	-	pA
Input Offset Current(1)	I_{OS}		-	±10	-	pA
NOISE PERFORMANCE						
Input Voltage Noise	e_np-p	f=0.01Hz to 10Hz	-	3.2	-	μVpp
		f=0.01Hz to 1Hz	-	0.97	-	μVpp
Input Voltage Noise Density	e_n	f=1KHz	-	140	-	nV/√Hz
Input Current Noise Density	i_n	f=10Hz	-	15	-	fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		-0.1	-	0.1	V
Common-Mode Rejection Ratio	CMRR	(V–)–0.1V<V_{CM}< (V+) + 0.1V	110	130	-	dB
INPUT CAPACITANCE						
Differential			-	1	-	pF
Common-Mode			-	5	-	pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L=10KΩ, V_O=0.3V ~ 4.7V, T_A= -40°C ~ +125°C	110	130	-	dB
DYNAMIC PERFORMANCE						
Slew Rate(5)	SR	G=+1	-	0.17	-	V/μs
Gain-Bandwidth Product	GBW		-	350	-	KHz
Overload Recovery Time	t_{OR}		-	6	-	us
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L=100 KΩ to GND	4.99	4.998	-	V
		R_L=10KΩ to GND	4.95	4.98	-	V
Output Voltage Low	V_{OL}	RL=100 KΩ to V+	-	1	10	mV
		RL=10 KΩ to V+	-	10	30	mV
Short-Circuit Current(3)(4)	I_{SC}		-	25	-	mA
POWER SUPPLY						
Operating Voltage Range	V_S		2.3	-	5.5	V
Quiescent Current/Amplifier	IQ		-	60	87	μA

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) Positive current corresponds to current flowing into the device.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(4) Short circuit test is a momentary test.

(5) Number specified is the slower of positive and negative slew rates.

TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = 25℃, Vs=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted

Fig 1. Offset Voltage Production Distribution

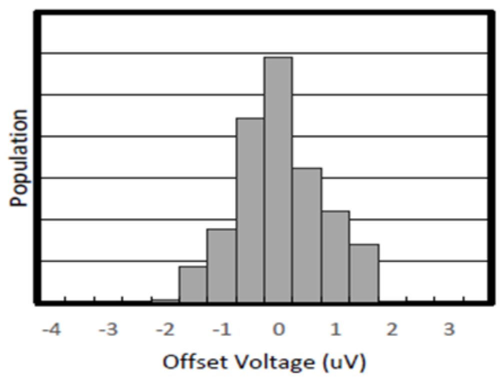


Fig 2. Offset Voltage Production Distribution

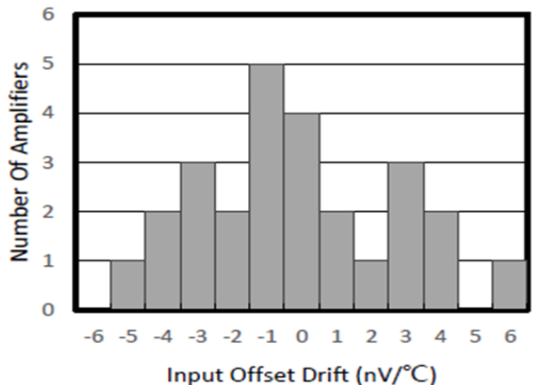


Fig 3. Open-Loop Gain and Phase vs. Frequency

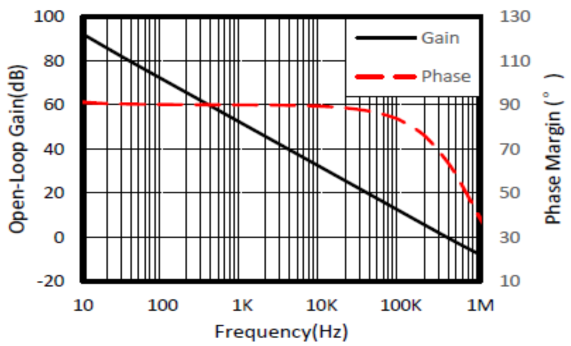


Fig 4. Input Bias Current vs. Temperature

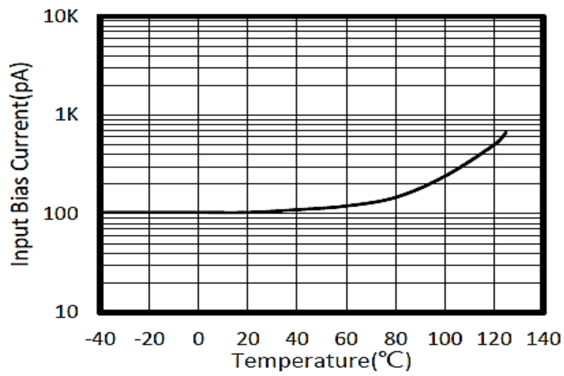


Fig 5. Power-Supply Rejection Ratio vs. Frequency

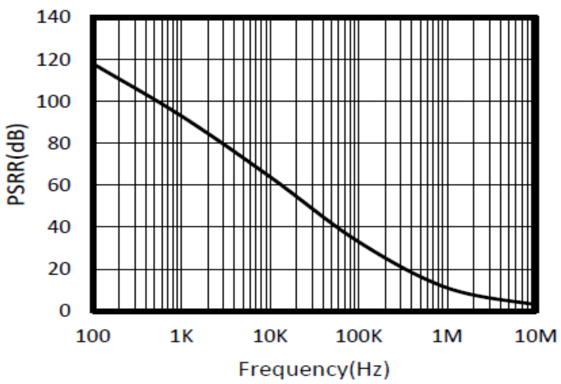


Fig 6. Common-Mode Rejection Ratio vs. Frequency

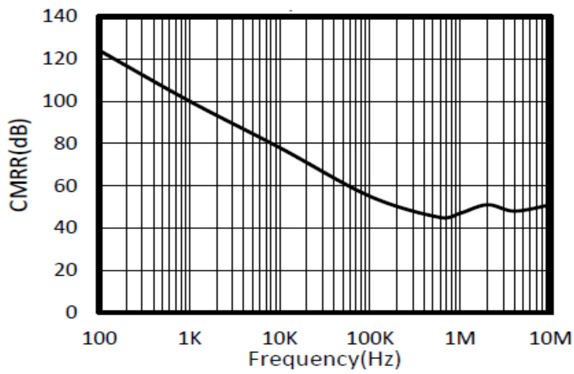


Fig 7. Quiescent Current vs. Temperature

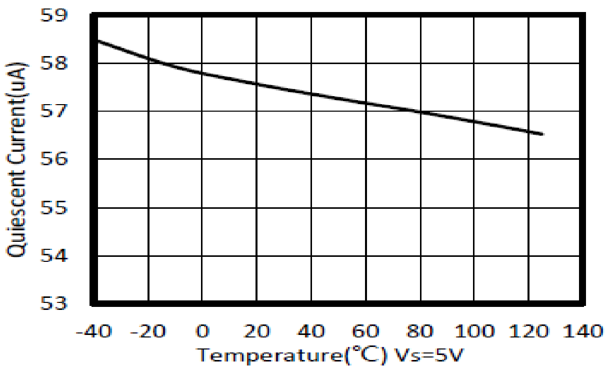


Fig 8. Quiescent Current vs. Temperature

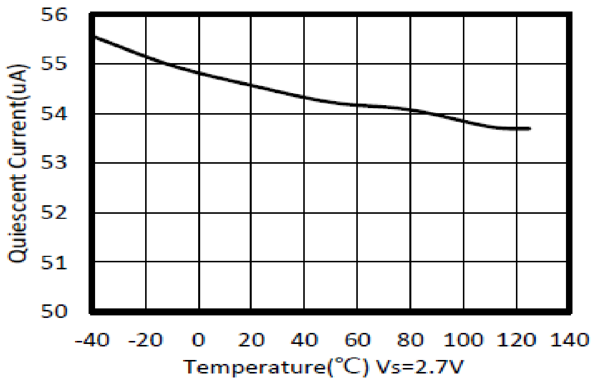


Fig 9. Sink Current vs. Temperature

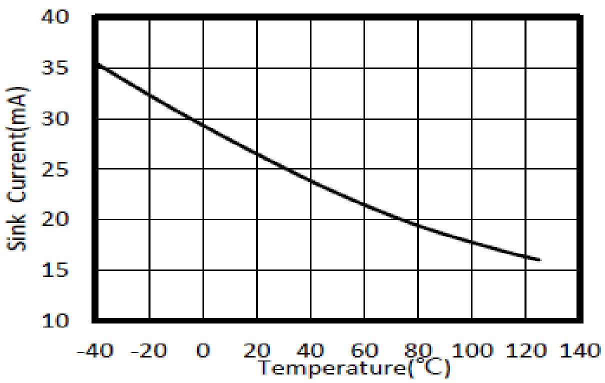


Fig 10. Source Current vs. Temperature

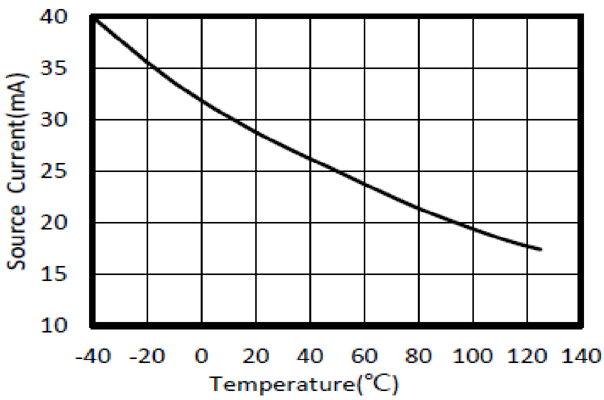


Fig 11. Small-Signal Step Response

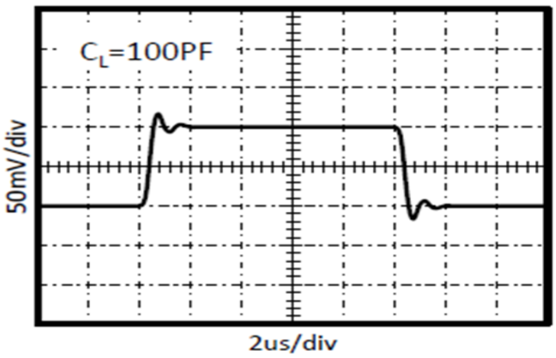


Fig 12. Large-Signal Step Response

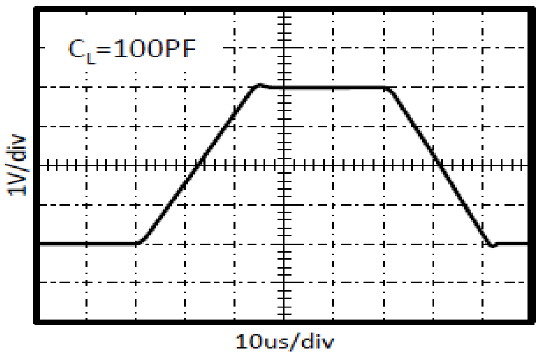


Fig 13. Positive Overvoltage Recovery

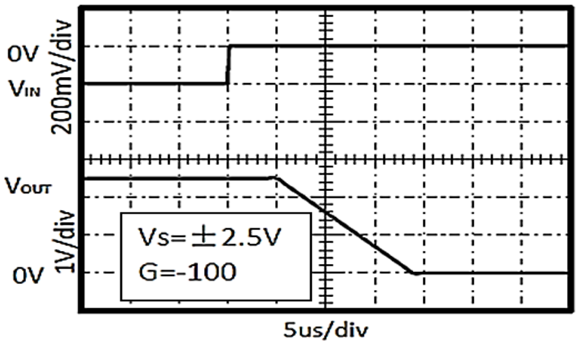


Fig 14. Negative Overvoltage Recovery

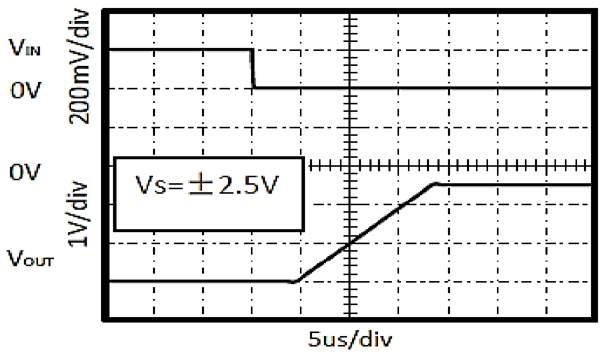


Fig 15. 0.01Hz to 10Hz Noise at V_S=5V

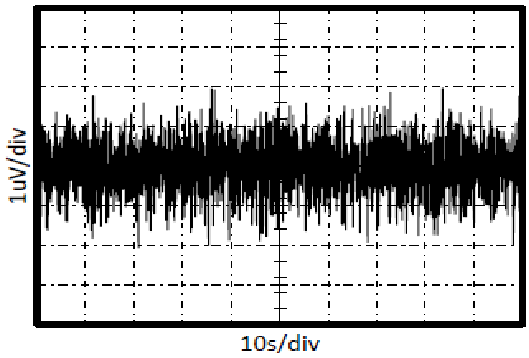


Fig 16. 0.01Hz to 10Hz Noise at V_S=2.7V

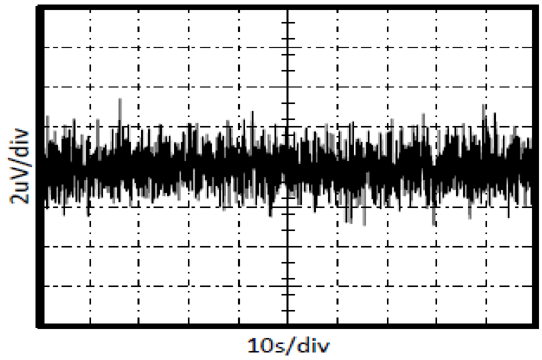


Fig 17. 0.01Hz to 1Hz Noise at V_S=5V

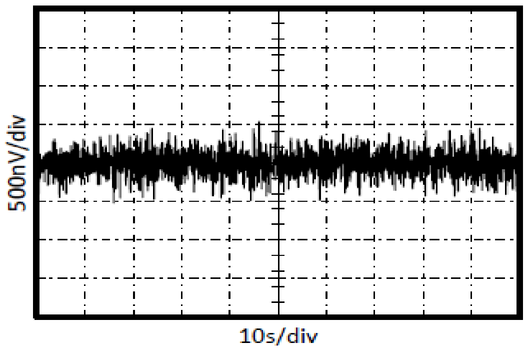
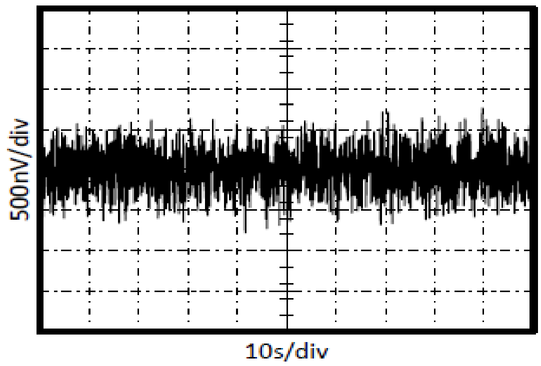
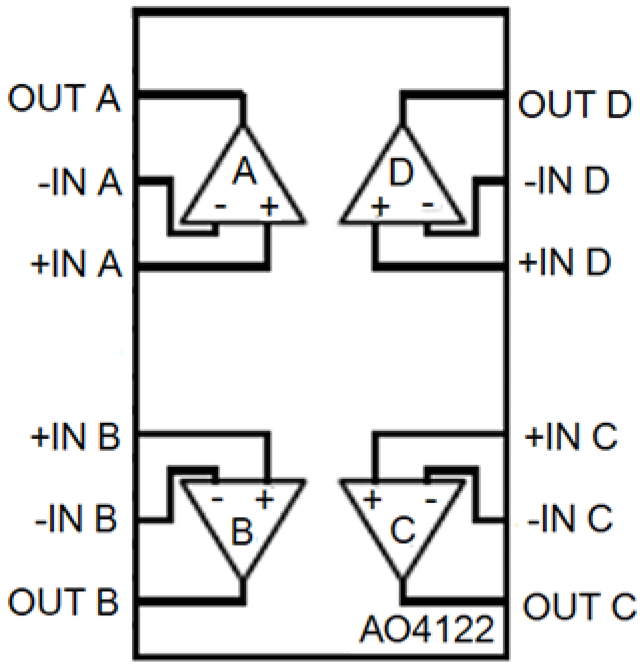


Fig 18. 0.01Hz to 1Hz Noise at V_S=2.7V



BLOCK DIAGRAM



DETAILED INFORMATION

Application Notes

The AO4122 is unity-gain stable and free from unexpected output phase reversal op amp. It use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature. Good layout practice mandates use of a 0.1μF capacitor practice mandates use of a 0.1μF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (See beck) effects in thermocouple junctions formed form connecting dissimilar conductor. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use Low Thermoelectric-Coefficient Connections (avoid dissimilar metals).
- Thermally Isolate Components Form Power Supplies or other Heat-Sources
- Shield Op Amp and input Circuitry form Air Currents, such as cooling fans.

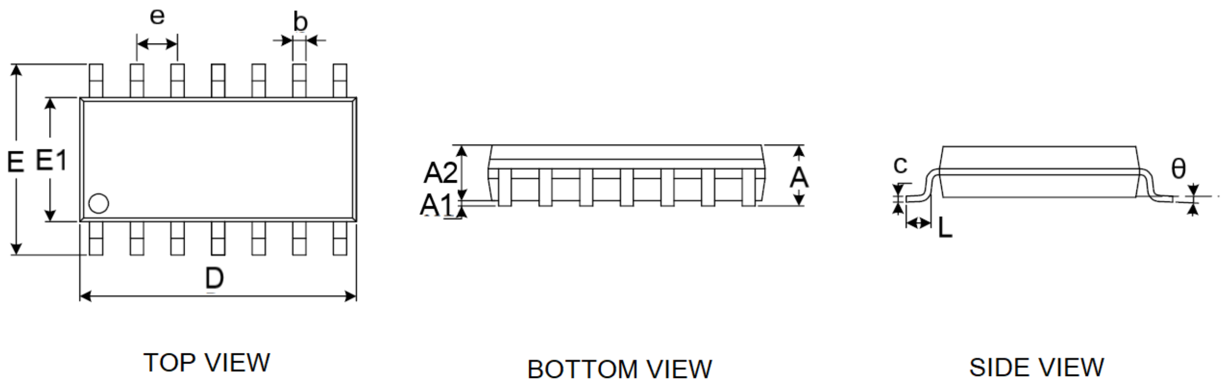
Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

Operating Voltage

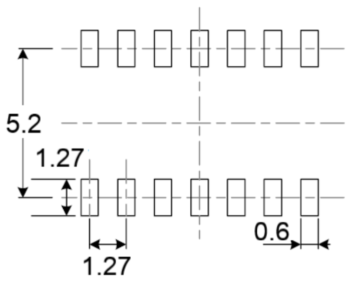
The AO4122 operates over a power-supply range of 2.3V to +5.5V (±1.15V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier.

PACKAGE INFORMATION

Dimension in SOP14 (Unit: mm)

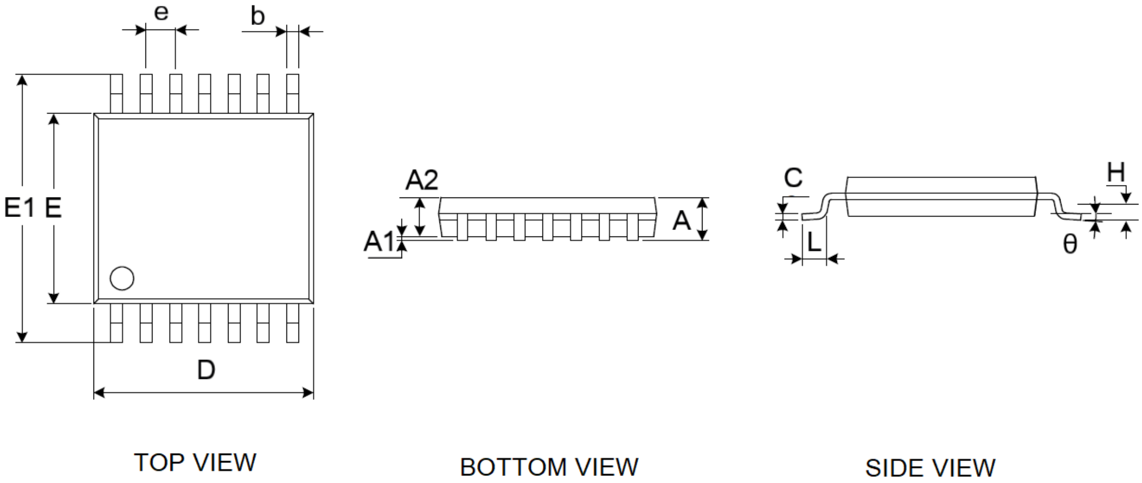


Recommended Land Pattern

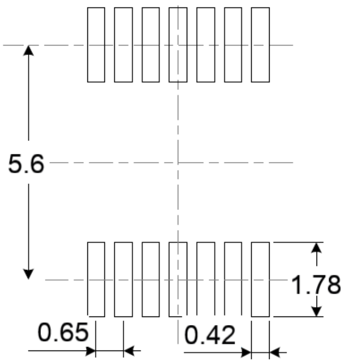


Symbol	Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.800	5.000
e	1.270 BSC	
E	5.800	6.200
E1	3.800	4.000
L	0.400	1.270
θ	0°	8°

Dimension in TSSOP14 (Unit: mm)



Recommended Land Pattern



Symbol	Millimeters	
	Min	Max
A	-	1.200
A1	0.50	0.150
A2	0.800	1.050
b	0.190	0.300
c	0.090	0.200
D	4.860	5.100
E	4.300	4.500
E1	6.250	6.550
e	0.650 BSC	
L	0.500	0.700
H	0.25 TYP	
θ	1°	7°

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