DESCRIPTION

The A25C256 is Electrically Erasable Programmable Memory (EEPROM) organized as 32768 x 8 bits, accessed through the SPI bus.

The A25C256 can operate with a supply range from 1.7V to 5.5V.

The A25C256 is available in SOP8, TSSOP8 and DFN8 Packages.

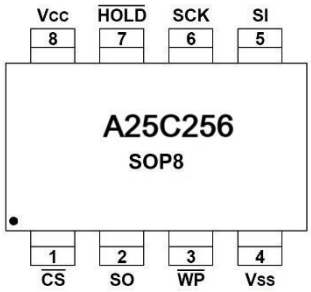
ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ:2,500pcs/Reel	M8	A25C256M8R-X
		A25C256M8VR-X
TSSOP8 SPQ: 3,000pcs/Reel	TMX8	A25C256TMX8R-X
		A25C256TMX8VR-X
DFN8 SPQ: 3,000pcs/Reel	J8	A25C256J8R-X
		A25C256J8VR-X
Note	X: Temperature A : -40℃ to +85℃ B : -40℃ to +105℃ C : -40℃ to +125℃: Halogen Free Package R: Tape & Reel	
AiT provides all RoHS products		

FEATURES

- Serial Peripheral Interface (SPI) data Transfer Protocol.
- Memory Array:
  256 Kbits (32 Kbytes) of EEPROM
  Page size: 64 Bytes.
- Single Supply Voltage and High Speed:
  1.7 V – 2.5 V 5 MHz
  2.5 V – 5.5 V 15 MHz
- Random and Sequential Read Modes.
- Write:
  Write within 3ms
  Partial Page Writes Allowed
- Write Protect: Quarter, Half or Whole Memory Array.
- High-Reliability
  Endurance: 4 Million Write Cycles
  Data Retention: 100 Years
- Enhanced ESD/Latch-up Protection:
  HBM 8000V
  Available in SOP8, TSSOP8 and DFN8 Packages.

PIN DESCIPTION



SOP8, M8

Top View

TSSOP8, TMX8

Top View

DFN8, J8

Top View

Pin # SOP8 / TSSOP8 / DFN8	Symbol	Type	Functions
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect
4	V_{SS}	P	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold
8	V_{CC}	P	Power Supply

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65℃ ~ +150℃
Voltage on any Pin with Respect to Ground *	-0.5V ~ +6.5V
V_{ESD}（HBM）	8000V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

RELIABILITY CHARACTERISTICS (2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_{END} (1)(2)	4,000,000	-	-	Program/Erase Cycles
Data Retention	T_{DR}	100	-	-	Years

(1) Page Mode, V_{CC} = 5 V, 25°C.

(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, unless otherwise specified.

A25C256-A	T_A = -40℃ ~ +85℃	V_{CC} = +1.7V to +5.5V
A25C256-B	T_A = -40℃ ~ +105℃	
A25C256-C	T_A = -40℃ ~ +125℃	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current (Read Mode)	I_{CCR}	Read, SO open f_{SCK} = 5MHz, 1.7V < V_{CC} < 2.5V	-	-	1.2	mA
		Read, SO open f_{SCK} = 15MHz, 2.5V < V_{CC} < 5.5V	-	-	1.8	
Supply Current (Write Mode)	I_{CCW}	Write, $\overline{CS}$= V_{CC}, 1.7V < V_{CC} < 5.5V	-	-	3	mA
Standby Current	I_{SB1}*	V_{IN} = GND or V_{CC}, $\overline{CS}$= V_{CC}, $\overline{WP}$= V_{CC}, $\overline{HOLD}$= V_{CC}, V_{CC} = 5.5 V	-	-	1	µA
Standby Current	I_{SB2}*	V_{IN} = GND or V_{CC}, $\overline{CS}$= V_{CC}, $\overline{WP}$= GND, $\overline{HOLD}$= GND, V_{CC} = 5.5 V	-	-	3	µA
Input Leakage Current	I_L	V_{IN} = GND or V_{CC}	-	-	±2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$= V_{CC}, V_{OUT} = GND or V_{CC}	-	-	±2	µA
Input Low Voltage	V_{IL1}	V_{CC} ≥ 1.7V	-0.45	-	0.3 V_{CC}	V
Input High Voltage	V_{IH1}	V_{CC} ≥ 1.7V	0.7 V_{CC}	-	V_{CC}+1	V
Output Low Voltage	V_{OL1}	V_{CC}= 2.5V, I_{OL} = 1.5mA, or V_{CC} = 5V, I_{OL} = 2mA	-	-	0.4	V
Output High Voltage	V_{OH1}	V_{CC}= 2.5V, I_{OL} =-0.4mA, or V_{CC} = 5V, I_{OL} = -2mA	0.8 V_{CC}	-	-	V
Output Low Voltage	V_{OL2}	V_{CC} = 1.7 V, I_{OL} = 0.15 mA				
Output High Voltage	V_{OH2}	V_{CC} = 1.7 V, I_{OL} = -0.1 mA				

* AC Test Conditions: (1) Input Pulse Voltages: 0.3 V_{CC} to 0.7 V_{CC} (2) Input rise and fall times: ≤ 10 ns

(3) Input and output reference voltages: 0.5 V_{CC} (4) Output load: current source I_{OL} max/I_{OH} max; C_L = 30 pF

AC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 1.7 V to 5.5 V, unless otherwise specified.

A25C256-A	T_A = -40℃ ~ +85℃	V_{CC} = +1.7V to +5.5V
A25C256-B	T_A = -40℃ ~ +105℃	
A25C256-C	T_A = -40℃ ~ +125℃	

Parameter	Symbol	1.7V ≤ V_{CC} < 2.5V			VCC ≧ 2.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_{SCK}	DC	-	5	DC	-	1	MHz
Data Setup Time	t_{SU}	20	-	-	10	-	-	ns
Data Hold Time	t_H	20	-	-	10	-	-	ns
SCK High Time	t_{WH}	80	-	-	40	-	-	ns
SCK Low Time	t_{WL}	80	-	-	40	-	-	ns
$\overline{HOLD}$ to Output Low Z	t_{LZ}	-	-	80	-	-	40	ns
Input Rise Time	t_{RI} (2)	-	-	2	-	-	1	μs
Input Fall Time	t_{FI} (2)	-	-	2	-	-	1	μs
$\overline{HOLD}$ Setup Time	t_{HD}	0	-	-	0	-	-	ns
$\overline{HOLD}$ Hold Time	t_{CD}	10	-	-	10	-	-	ns
Output Valid from Clock Low	t_V	-	-	80	-	-	40	ns
Output Hold Time	t_{HO}	0	-	-	0	-	-	ns
Output Disable Time	t_{DIS}	-	-	80	-	-	40	ns
$\overline{HOLD}$ to Output High Z	t_{HZ}	-	-	80	-	-	40	ns
$\overline{CS}$ High Time	t_{CS}	90	-	-	40	-	-	ns
$\overline{CS}$ Setup Time	t_{CSS}	60	-	-	30	-	-	ns
$\overline{CS}$ Hold Time	t_{CSH}	60	-	-	30	-	-	ns
$\overline{CS}$ Inactive Setup Time	t_{CNS}	60	-	-	30	-	-	ns
$\overline{CS}$ Inactive Hold Time	t_{CNH}	60	-	-	30	-	-	ns
$\overline{WP}$ Setup Time	t_{WPS}	10	-	-	10	-	-	ns
$\overline{WP}$ Hold Time	t_{WPH}	10	-	-	10	-	-	ns
Write Cycle Time	t_{WC}(3)	-	-	5	-	-	5	ms

(1) AC Test Conditions:
Input Pulse Voltages: 0.3 V_{CC} to 0.7 V_{CC}
Input rise and fall times: ≤ 10 ns
Input and output reference voltages: 0.5 V_{CC}
Output load: current source I_{OL} max/I_{OH} max; C_L = 30 pF

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

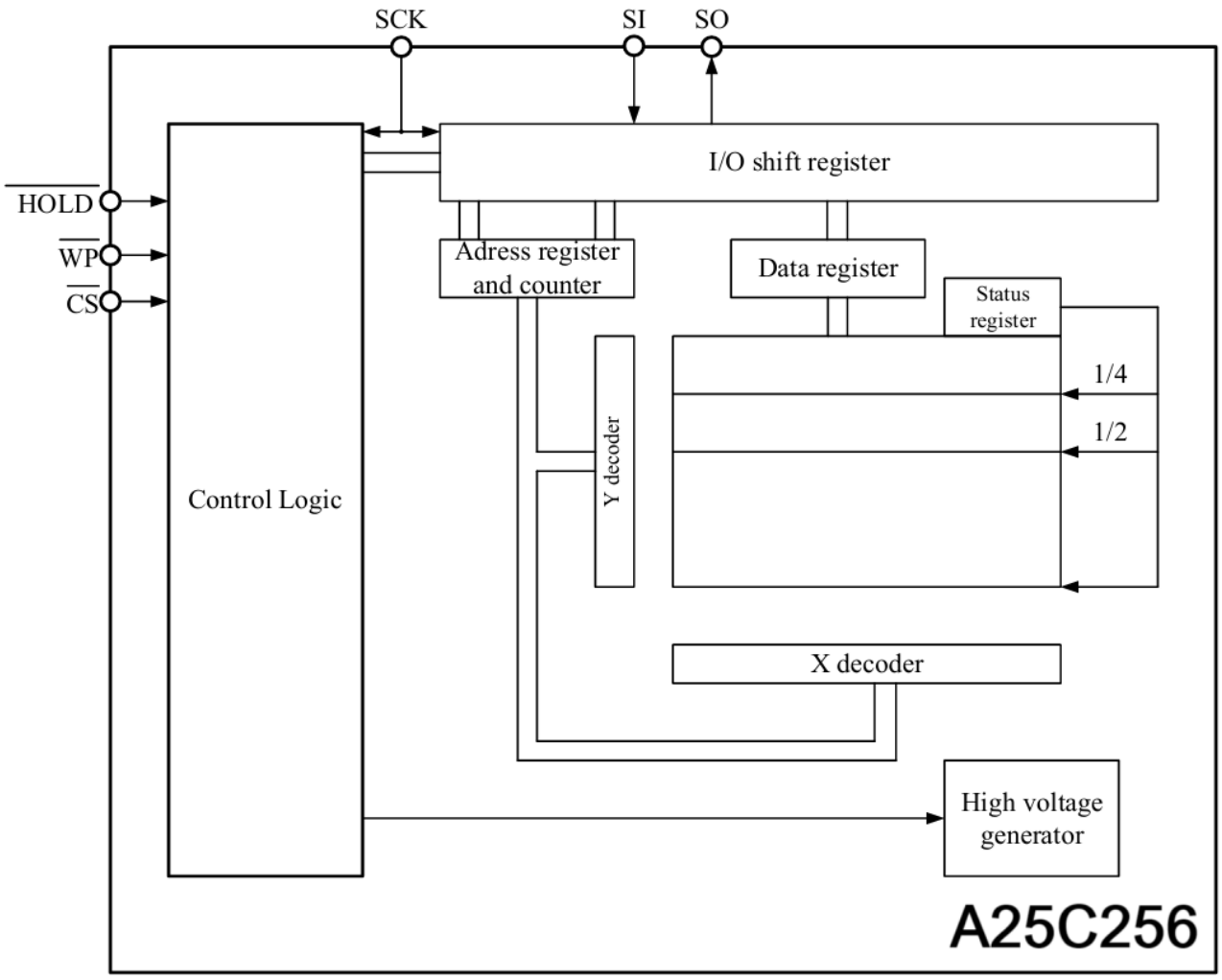
POWER-UP TIMING (1)(2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-up to Read	t_{PUR}	-	-	-	0.1	ms
Write Operation	t_{PUW}	-	-	-	0.1	ms

(1) This parameter is tested initially and after a design or process change that affects the parameter.

(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated

BLOCK DIAGRAM



DETAILED INFORMATION

Serial Data Input (SI): The SPI Serial data input (SI) is used to serially receive write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) input pin.

Serial Data Output (SO): The SPI Serial data output (SO) is used to read data or status from the device on the falling edge of CLK.

Serial Clock (SCK): The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations.

Chip Select ($\overline{CS}$): The SPI Chip Select ($\overline{CS}$) pin enables and disables device operation. When ($\overline{CS}$) is high, the device is deselected and the Serial Data Output (SO) pins are at high impedance. When deselected, the device power consumption will be at standby levels unless an internal write cycle is in progress. When ($\overline{CS}$) is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, ($\overline{CS}$) must transition from high to low before a new instruction will be accepted.

Hold ($\overline{HOLD}$): The $\overline{HOLD}$ pin allows the device to be paused while it is actively selected. When $\overline{HOLD}$ is brought low, while $\overline{CS}$ is low, the SO pin will be at high impedance and signals on the SI and SCK pins will be ignored (don't care). When $\overline{HOLD}$ is brought high, device operation can resume. The $\overline{HOLD}$ function can be useful when multiple devices are sharing the same SPI signals. The $\overline{HOLD}$ pin is active low.

Write Protect ($\overline{WP}$): The Write Protect ($\overline{WP}$) pin is used in conjunction with the Status Register Write Disable (SRWD) Bit to prevent the Status Registers from being written. Write Protect ($\overline{WP}$) pin and Status Register Write Disable (SRWD) Bit enable the device to be put in the Hardware Protected mode (when Status Register Write Disable (SRWD) Bit is set to 1, and Write Protect ($\overline{WP}$) pin is driven low.

FUNCTION DESCRIPTION

The A25C256 supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The A25C256 contains an 8−bit instruction register. The instruction set and associated op−codes are listed in Table 1.

Reading data stored in the A25C256 is accomplished by simply providing the READ command and an address. Writing to the A25C256, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the A25C256 will accept any one of the six-instruction op−codes listed in Table 1 and will ignore all other possible 8−bit combinations. The communication protocol follows the timing from Figure 10.

Table 1

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

1.Status Register

The Status Register, as shown in Table 2, contains a number of status and control bits.

Table 2

7	6	5	4	3	2	1	0
SRWD	1	1	1	BP1	BP0	WEL	$\overline{READY}$

$\overline{READY}$: The $\overline{READY}$ bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

BP0, BP1: The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non−volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 3. The protected blocks then become read−only.

Table 3

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	6000h−7FFFh	Quarter Array Protection
1	0	4000h−7FFFh	Half Array Protection
1	1	0000h−7FFFh	Full Array Protection

SRWD: The SRWD (Status Register Write Disable) bit acts as an enable for the WP pin. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the SRWD bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non−block protected memory can be written. Hardware write protection is disabled when the $\overline{WP}$ pin is high or the SRWD bit is 0. The SRWD bit, WP detailed in Table 4.

Table 4

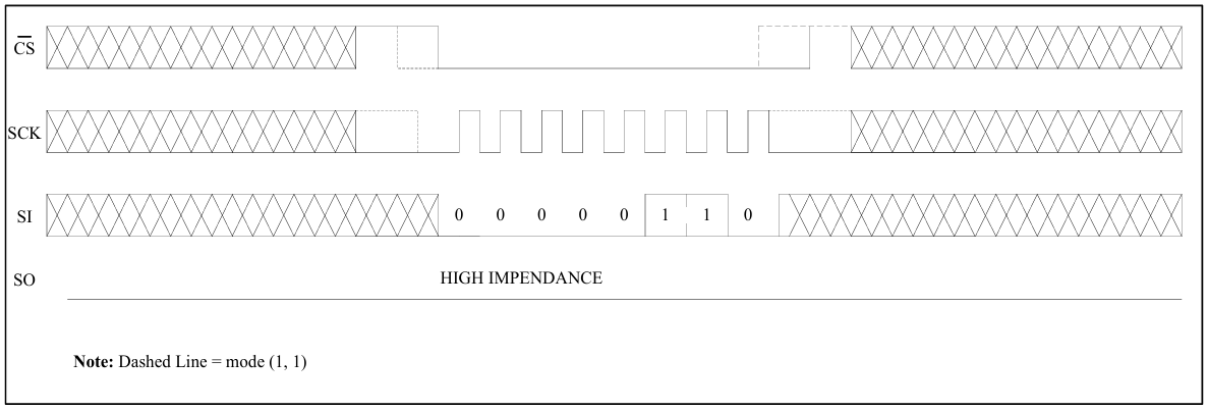
SRWD	WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

2. Write Operations

The A25C256 powers up into a write disables state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

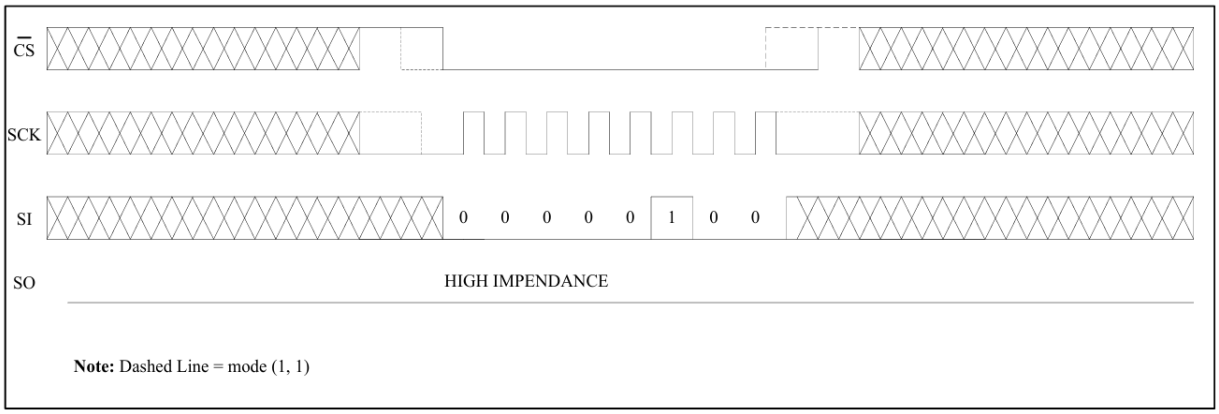
Write Enable and Write Disable: The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the A25C256. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 1. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

Figure 1



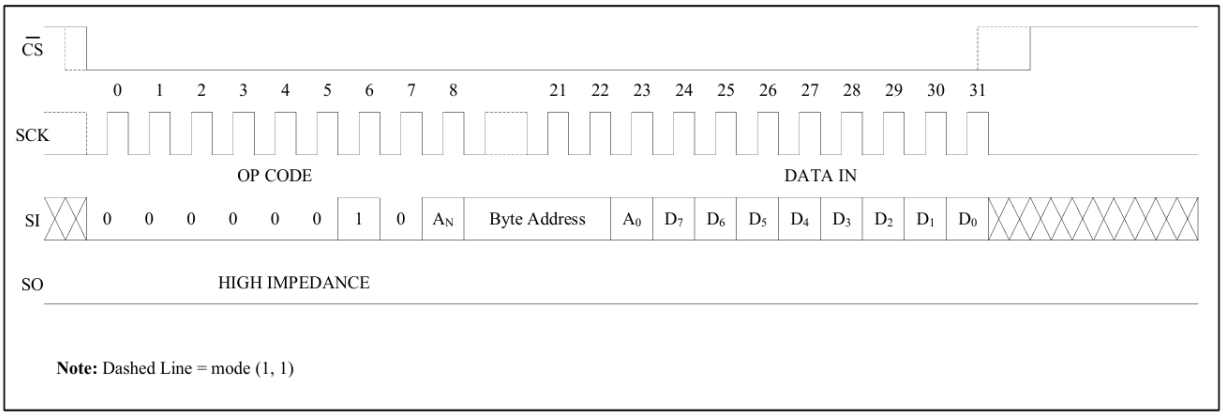
The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 2. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

Figure 2



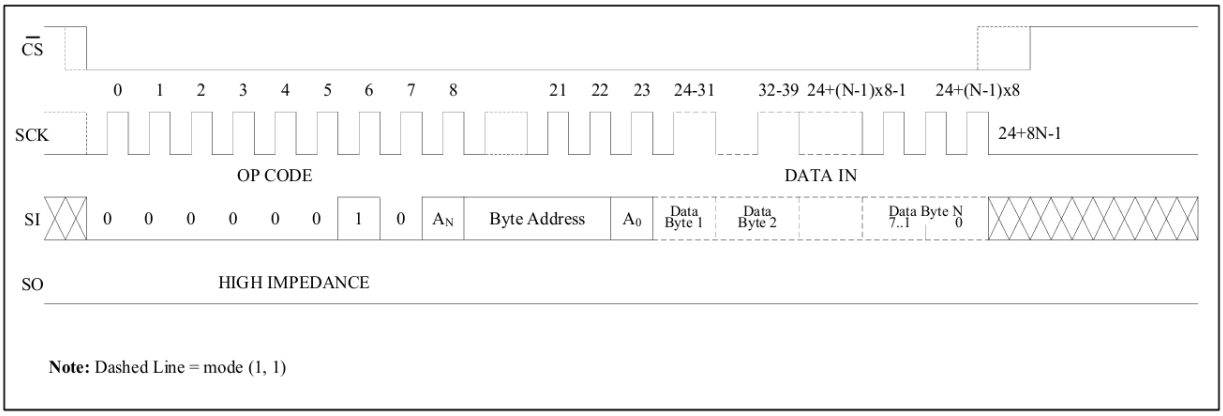
Byte Write: Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16−bit address and a data byte as shown in Figure 3. Only 8 Significant address bits are used by the A25C256. The rest are don't care bits. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{READY}$ bit will indicate if the internal write cycle is in progress ($\overline{READY}$ high), or the device is ready to accept commands ($\overline{READY}$ low).

Figure 3



Page Write: After sending the first data byte to the A25C256, the host may continue sending data, up to a total of 64 bytes, according to timing shown in Figure 4. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will “roll over” to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the A25C256 is automatically returned to the write disable state.

Figure 4

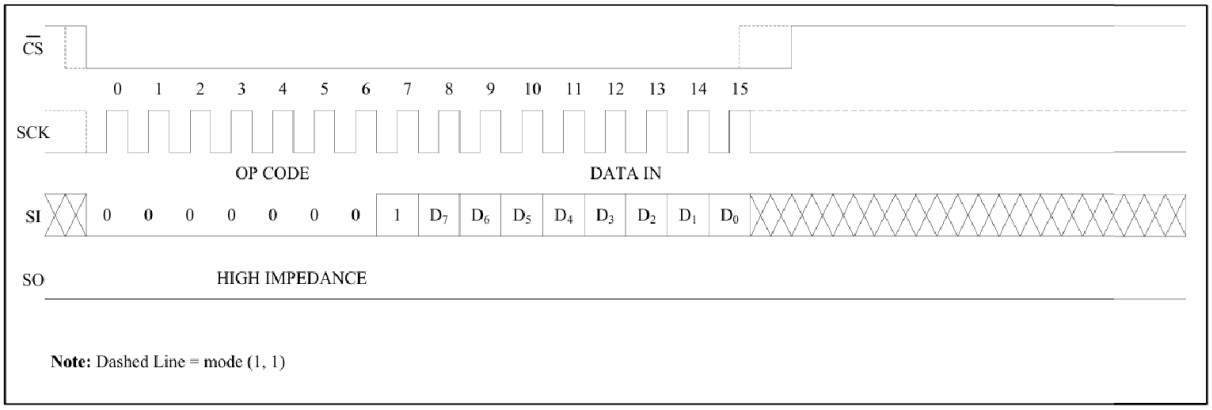


Write Status Register: The Status Register is written by sending a WRSR instruction according to timing shown in Figure 5. Only bits 2 and 3 can be written using the WRSR command.

Figure 5

Device	Address Significant Bits	Address Don’t Care Bits	Address Clock Pulses
Main Memory Array	A14-A0	A15	16

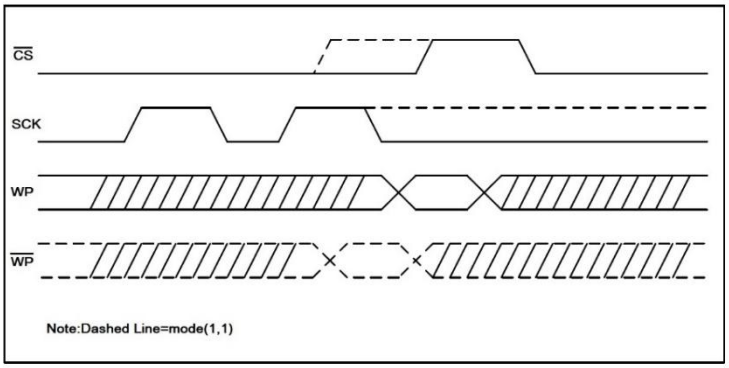
Figure 5



Write Protection: The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against

being inadvertently altered. When ($\overline{WP}$) is low, write operations to the Status Register are inhibited. ($\overline{WP}$) going low while ($\overline{CS}$) is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, ($\overline{WP}$) going low will have no effect on any write operation to the Status Register. The ($\overline{WP}$) pin function is blocked when the SRWD bit is set to “0”. The ($\overline{WP}$) input timing is shown in Figure 6.

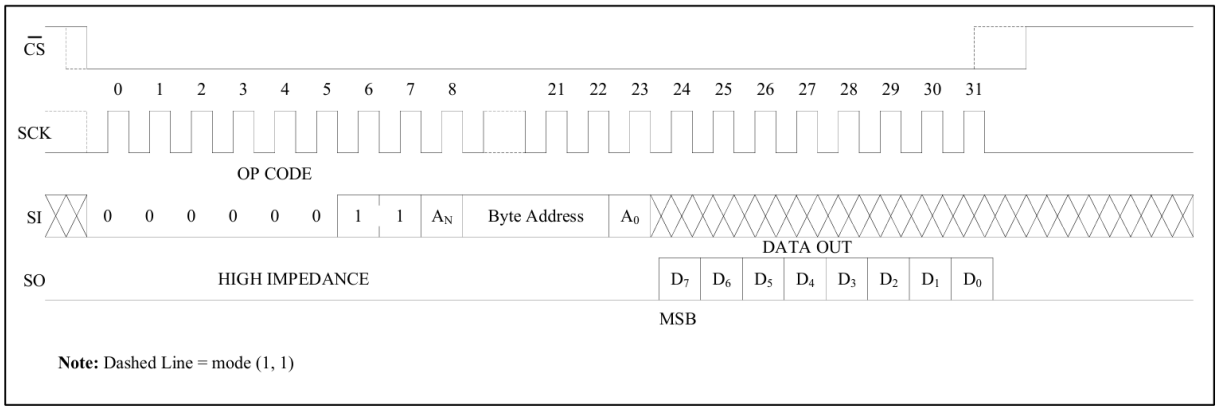
Figure 6



3. Read Operations

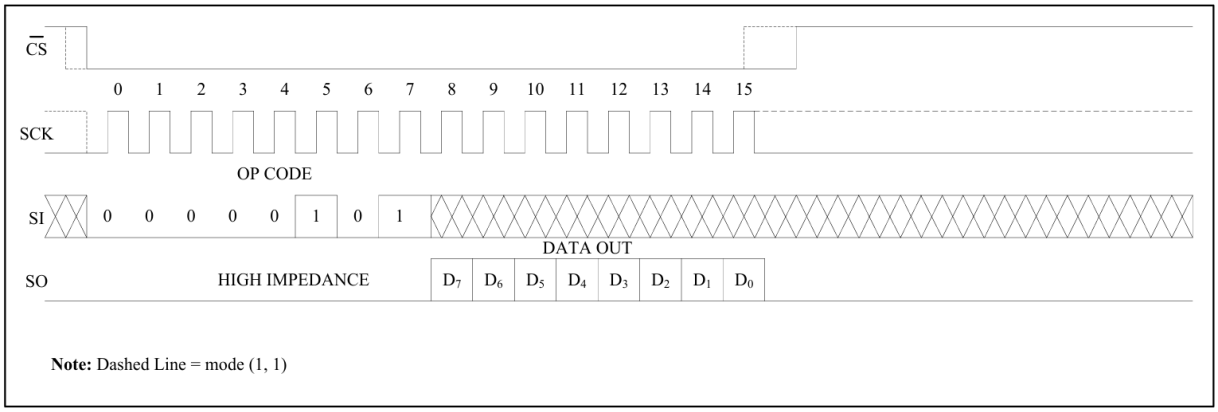
Read from Memory Array: To read from memory, the host sends a READ instruction followed by a 8−bit address. After receiving the last address bit, the A25C256 will respond by shifting out data on the SO pin (as shown in Figure 7). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Figure 7



Read Status Register: To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the A25C256 will shift out the contents of the status register on the SO pin (Figure 8). The status register may be read at any time, including during an internal write cycle.

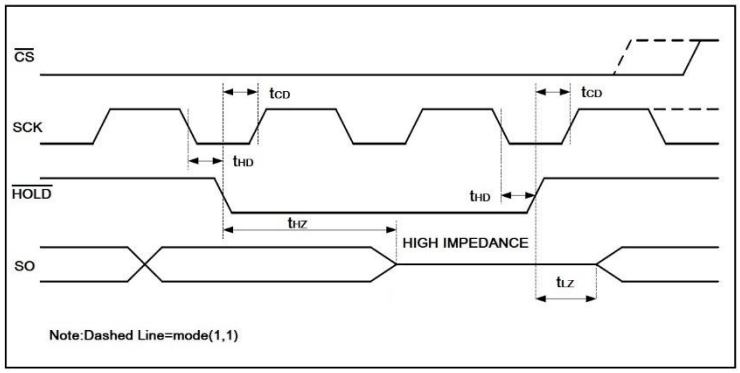
Figure 8



4. Hold Operation

The $\overline{HOLD}$ input can be used to pause communication between host and A25C256. To pause, $\overline{HOLD}$ must be taken low while SCK is low (Figure 9). During the hold condition the device must remain selected ($\overline{CS}$ low). During the pause, the data output pin (SO) is tri−stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{HOLD}$ must be taken high while SCK is low.

Figure 9



5. Design Considerations

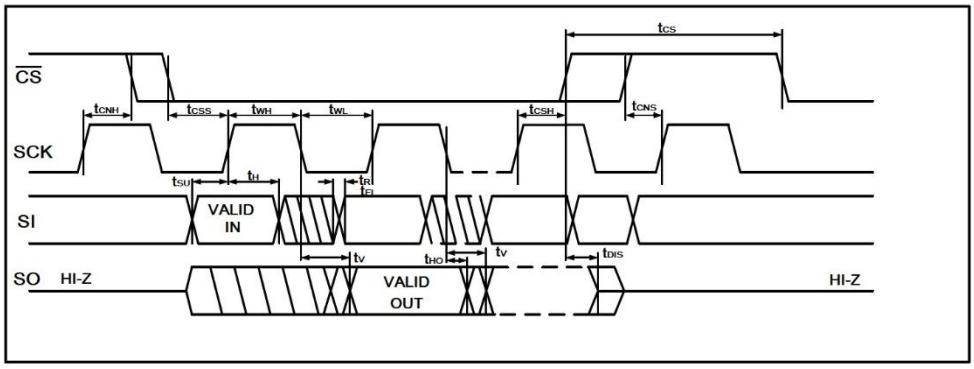
The A25C256 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the device against 'brown−out' failure following a temporary loss of power.

The A25C256 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the $\overline{CS}$ pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The $\overline{CS}$ input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op−code will be ignored and the serial output pin (SO) will remain in the high impedance state.

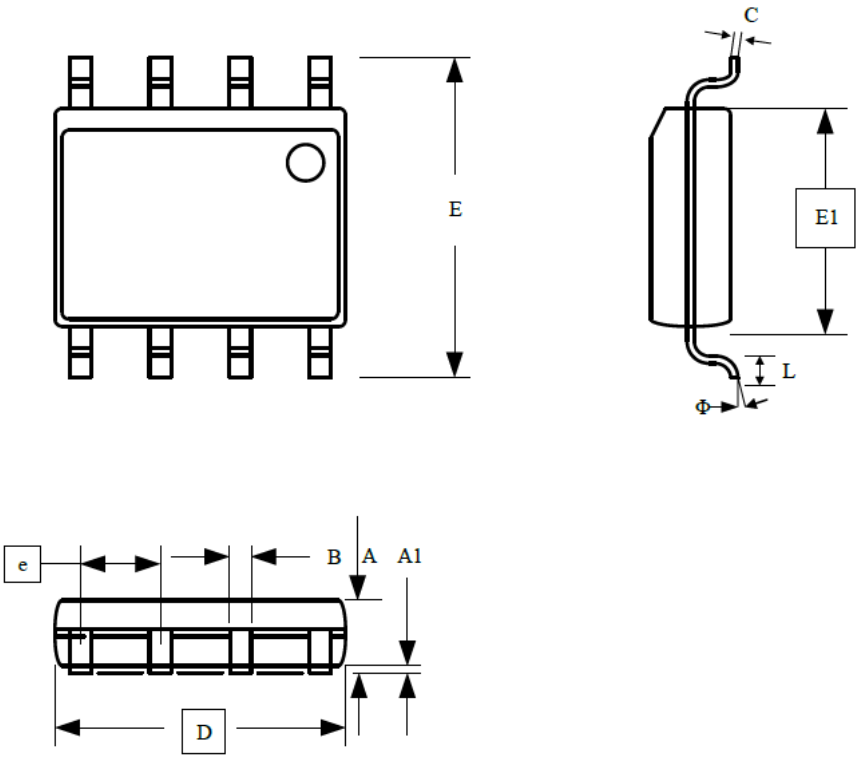
BUS TIMING

Figure 10



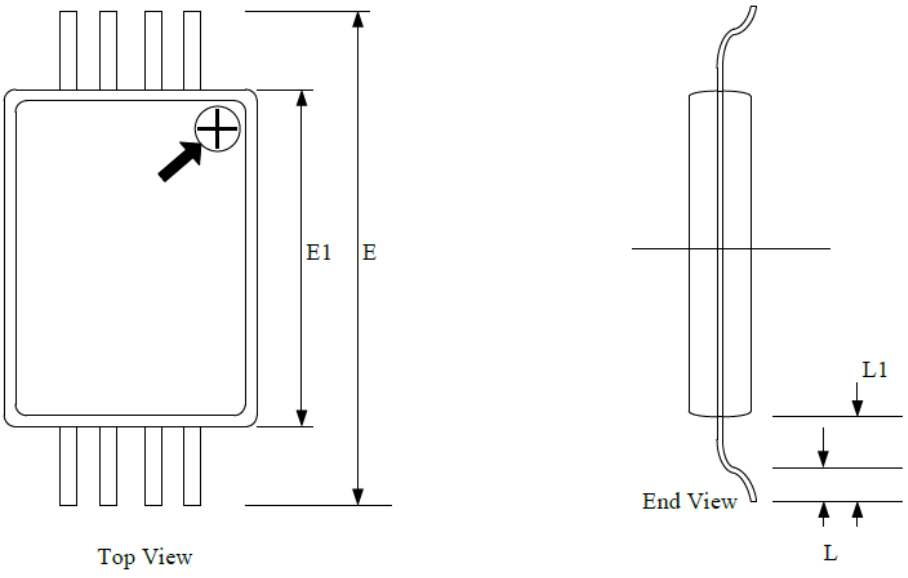
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



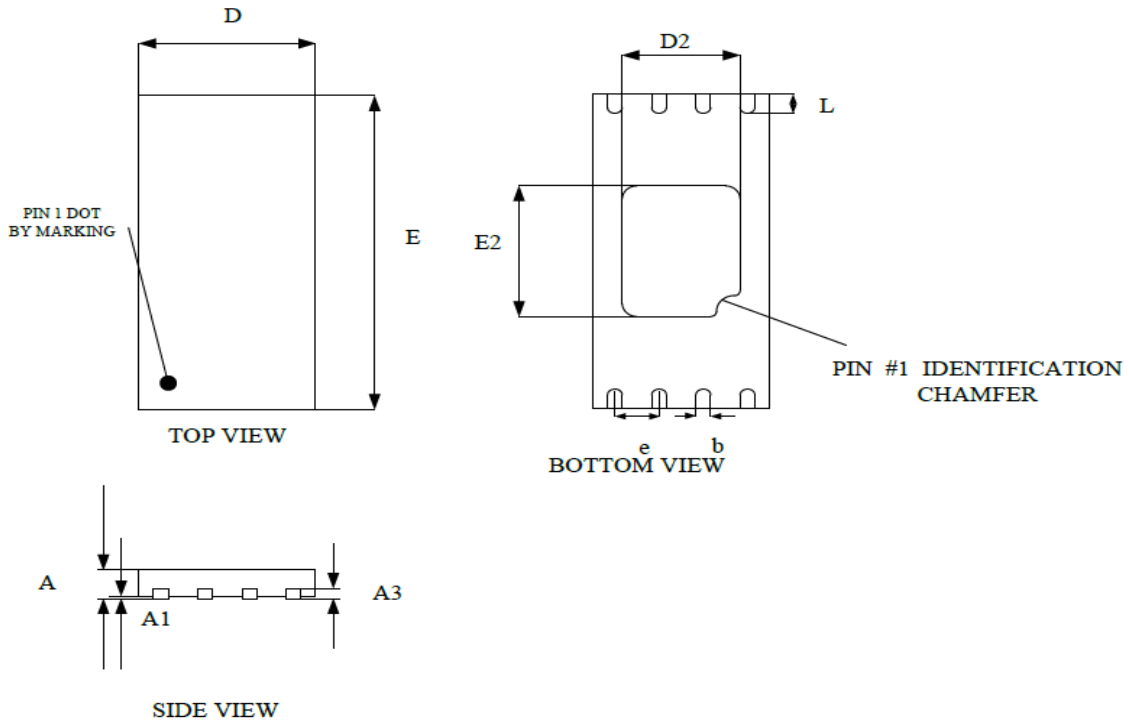
Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.230
B	0.390	0.480
C	0.210	0.260
D	4.700	5.100
E1	3.700	4.100
E	5.800	6.200
e	1.270 BSC	
L	0.500	0.800
θ	0°	8°

Dimension in TSSOP8 Package (Unit: mm)



Symbol	Min	Max
D	2.900	3.100
E	6.200	6.600
E1	4.300	4.500
A	-	1.200
A1	0.050	0.150
b	0.210	0.300
e	0.650 BSC	
L	0.450	0.750
L1	1.000 REF	

Dimension in DFN8 (Unit: mm)



Symbol	Min	Max
A	0.500	0.600
A1	0.000	0.050
A3	0.152 REF	
D	1.900	2.100
E	2.900	3.100
b	0.200	0.300
L	0.250	0.350
D2	1.300	1.500
E2	1.200	1.400
e	0.500 BSC	

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