DESCRIPTION

The A7933 employs constant on-time (COT) control architecture, providing excellent transient response. This high-voltage, step-down switching regulator can deliver up to 3.2 Amps of continuous current to the load and features an integrated high-side, high-voltage power MOSFET with a typical current limit of 5 Amps. It operates within a broad input voltage range of 6.0V to 90V and has built-in soft-start functionality. The A7933 is ideal for various step-down applications, particularly in the automotive, industrial, and lighting sectors. Additionally, the device includes patented standby circuits that enable a quick transition from standby mode, reducing the need for external components. The switching frequency can go as high as 500 kHz, enabling the use of smaller components. Furthermore, features like thermal shutdown (OTP) and short-circuit protection (OCP) ensure reliable hiccup mode operation to protect both the circuitry and the IC. With a quiescent current of only 13 µA, the A7933 is ideal for power-saving applications in various systems. It also includes a 3.3V fixed output LDO that can supply up to 50 mA of output current, offering an additional power reference.

The A7933 is available in PSOP8 Packages.

ORDERING INFORMATION

Package Type	Part Number
PSOP8 SPQ: 4,000pcs/Reel	A7933MP8VR
Note	R: Tape & Reel V: Halogen free Package
AiT provides all RoHS products	

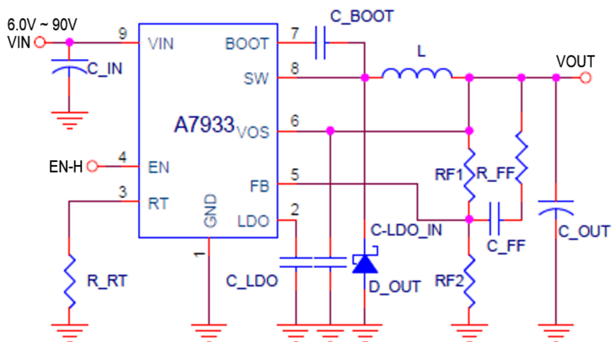
FEATURES

- Wide Input Voltage 6.0V–90V
- Up to 500Khz Switching
- PWM Control input for automotive, industrial, and lighting sectors application.
- Integrated 100mΩ High-Side MOSFET
- 13uA Quiescent Current
- Precision ±1% Feedback Reference
- Integrated 3.3V/50 mA LDO
- OCP, with OTP Thermal Shutdown
- PSOP8 Package with Thermal PAD

APPLICATION

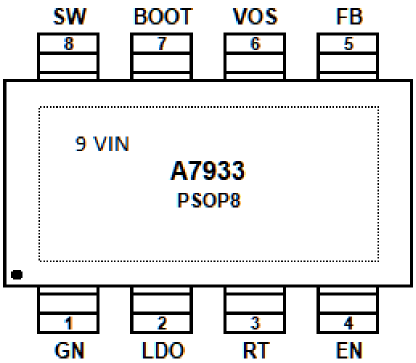
- Automotive and Industry Systems
- lighting sectors, Motor Drives and Telecom

TYPICAL PPLICATION



L : 22uH: WSL12050-220M
47uH: WSL12060-470M
68uH: WSL12060-680M
D_OUT: SM540C~SM5100C

PIN DESCRIPTION



PSOP8, MP8

Top View

PIN#	Symbol	I/O	Function
1	GND	Analog Input	Ground
2	LDO	Analog Power Output	3.3V LDO output, connect a capacitor to GND higher than 1uF; leave as float before device enabled to disable internal LDO.
3	RT	Analog Input	Connect a resistor to GND and set the switching frequency.
4	EN	Analog Input	Buck and LDO enable internal pull-down by 0.08μA. Source 2μA after device enabled. Connect to the VIN pin if the hysteresis function is not used.
5	FB	Analog Input	For feedback input, connect it to the output voltage resistor divider.
6	VOS	Analog Power Input	The output sense and internal LDO input connect to the output cap with 100mA current capability PCB trace; Place 0.1μF cap close to VOS pin.
7	BOOT	Analog Power Input	Boot-strap pin. Decouple this pin to the SW pin with >100nF (0.2V drop) ceramic capacitor.
8	SW	Analog Power Output	Connect to the switch node of the power inductor and a Schottky diode between this pin and GND.
9	VIN	Analog Power Input	Input pin. Decouple this pin to GND with a low ESR capacitor. Connect to a VIN power plane to improve thermal performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

VIN, EN, SW to END, Input Voltage	-0.3 ~ 92V
SW to GND (20ns pulse), Input Voltage	-3 ~ 92V
BOOT to GND, Input Voltage	-0.3 ~ 100V
FB, RT to GND, Input Voltage	-0.3 ~ 6.6V
VOS to GND, Input Voltage	-0.3 ~ 26V
I_D, Continuous Drain Current (1), T_C=25℃	4.8A
$I_{D,pulse}$ Pulsed drain current (2), T_C=25℃	21A
B_{VDSS}, Internal MOSFET Breakdown Voltage	100V
T_J, Operating Junction Temperature	-40 ~ 125℃
T_{stg}, Storage Temperature	-65 ~ 160℃
T_{SLD}, Soldering Temperature (10 second)	260℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Calculated continuous current based on maximum allowable junction temperature.

(2) Repetitive rating; pulse width limited by max. junction temperature.

ESD RATINGS

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDES JS-001(1)	±500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

(1) JEDEC document JEP155 states the 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states the 250V CDM allows safe manufacturing with a standard ESD control process

RECOMMENDED OPERATING CONDITIONS

		MIN.	MAX.	Units
Recommended Operation Conditions	VIN Voltage	6.0	90	V
	EN Voltage	-0.3	90	V
	SW Voltage	-0.3	90	V
	Ambient Temperature	-40	+125	℃

RECOMMENDED OPERATING CONDITIONS

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	30	℃/W
	θ_{JC} (Junction to case)	10	℃/W

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, V_{OUT}=12V, L=22µH, C_{OUT}=22µF, Typical values correspond to T_J=25℃, Minimum and Maximum limits apply over the full junction temperature range (-40℃ to 125℃) unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
INPUT VOLTAGE						
Input Voltage	V_{IN}	-	6.0	-	90	V
Input UVLO hysteresis	$V_{IN-UVLO}$	-	-	5.6	6.3	V
Input UVLO hysteresis	V_{IN-UVL_HYS}	-	-	0.6	-	V
SUPPLY CURRENT						
Shutdown Current	$I_{SHUTDOWN}$	V_{EN}=0V	-	12	30	µA
None Switching Quiet Current	I_Q	EN=V_{IN}, VOS higher than target, I_{LDO}=0A	-	13	-	µA
Standby Current	$I_{STANDBY}$	I_{OUT}=0A, I_{LDO}=0A	-	-	100	µA
FEEDBACK						
Feedback Reference Voltage	V_{REF}	-	1.205	1.22	1.235	V
EN						
EN Rising Threshold	V_{ENH}	V_{IN}=48A, I_{OUT}=0.1A	-	1.22	1.26	V
EN Falling Threshold	V_{ENL}	V_{IN}=48A, I_{OUT}=0.1A	1.17	1.2	-	V
Hysteresis Input Current	$I_{EN\_Hysteresis}$	V_{IN}=48A, I_{OUT}=0.1A	-	-2	-	µA
FREQUENCY (1)						
Programmable Switching Frequency Range	F_{SW}	F_{SW} (kHZ)=$\frac{22\times10^3}{RT(k\Omega)}$	-	-	500	KHz
LDO						
LDO Output Voltage	V_{LDO}	VOS=12V, 0mA – 50mA	3.2	3.3	3.4	V
LDO Over Current	I_{LDOOC}	VLDO=0V	-	55	-	mA
TIMING						
Minimum On-Time	t_{ON-MIN}	-	-	200	-	ns
Minimum Off-Time	$t_{OFF-MIN}$ (1)	-	-	200	-	ns
POWER SWITCHES						
High-side MOSFET RDSON	$R_{DSON-HS}$	T_A=25℃	-	100	-	mΩ
CURRENT LIMIT						
High-side MOSFET Peak Current Limit	$I_{PEAK-HS}$	-	-	4.8	-	A
SOFT START						
Soft-start Time	t_{SS}	V_{FB} for 0V to V_{REF}	-	3.5	-	ms
UVP Hiccup Time *	t_{Hiccup}	-	-	60	-	ms
UNDER VOLTAGE PROTECION						
UVP Falling Threshold	V_{UVPF}	V_{FB} Voltage	-	0.60	-	V
UVP Rising Threshold	V_{UVPR}	V_{FB} Voltage	-	0.62	-	V
THERMAIL SHUTDOWN (1)						
Thermal Shutdown Threshold	T_{SD}	T_J rising	-	150	-	℃
Thermal Shutdown Hysteresis	T_{HYS}	-	-	20	-	℃

*Values are verified by characterization on the bench, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=45V, V_{OUT}=12V, L=22μH, C_{OUT}=22μF, T_A=25℃, unless otherwise specified.

Fig 1. Efficiency at 12Vout

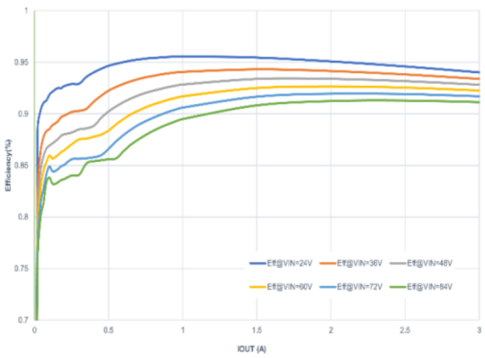


Fig 2. Load and Line Regulation

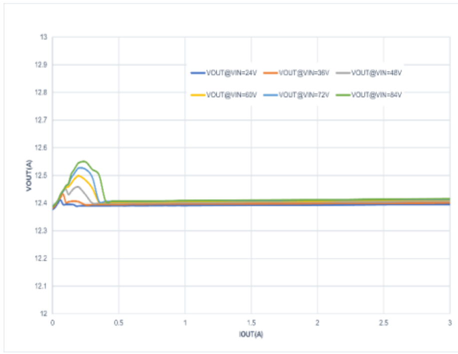
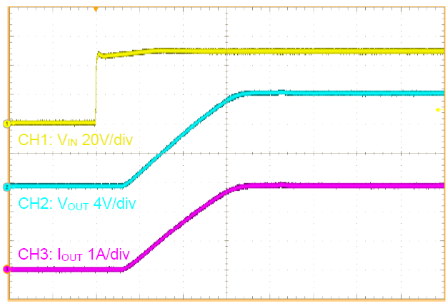
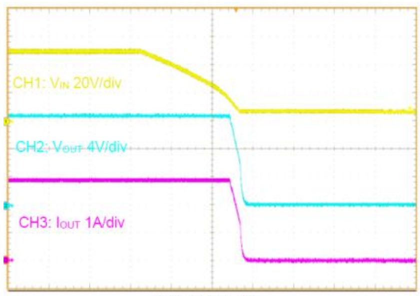


Fig 3. Startup from V_{IN}



Time(1ms/div)

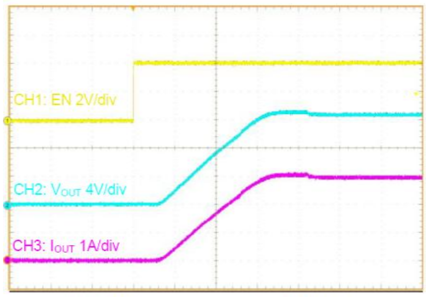
Fig 4. Shutdown from V_{IN}



Time(5ms/div)

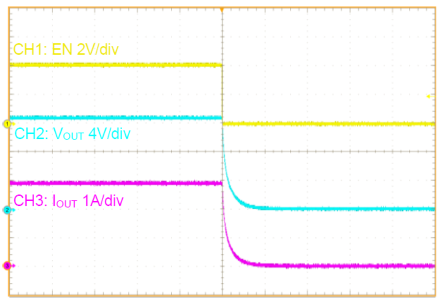
V_{IN}=48V, V_{OUT}=12V, L=22μH, C_{OUT}=22μF, T_A=25℃

Fig 5. Startup from EN



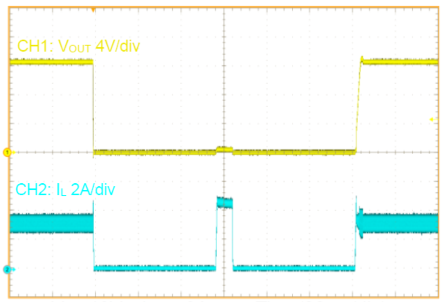
V_{IN}=48V Time(1ms/div)

Fig 6. Shutdown from EN



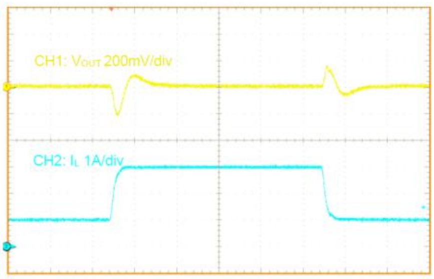
V_{IN}=48V Time(1ms/div)

Fig 7. Short Protection and Recovery



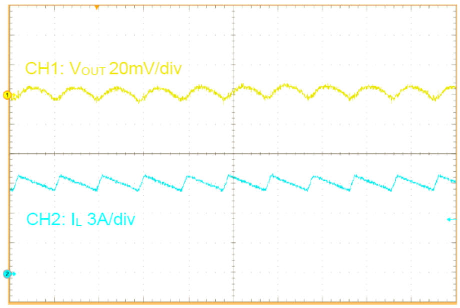
V_{IN}=48V I_{OUT}=3A Time(20ms/div)

Fig 8. Load Transient



V_{IN}=48V V_{OUT}=5V Time(1ms/div) I_{OUT}:1A ~ 3A,3A/us

Fig 9. Out Ripple



V_{IN}=48V V_{OUT}=5V Time(5μs/div) I_{OUT}=3A

Fig 10. VIN UVLO vs Temperature

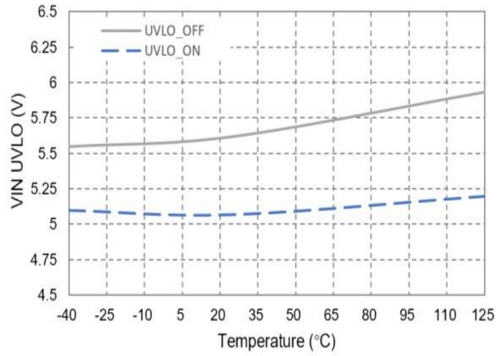


Fig 11. VEN vs Temperature

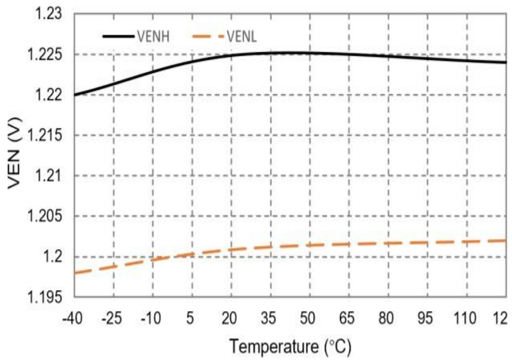


Fig 12. VREF vs Temperature

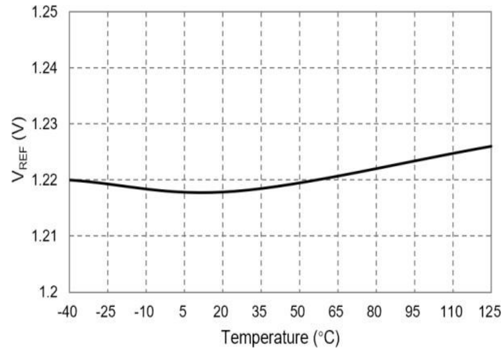


Fig 13. V_{LDO} vs Temperature

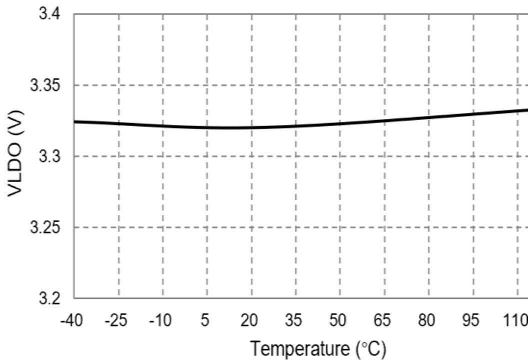


Fig 14. R_{dson} vs Temperature

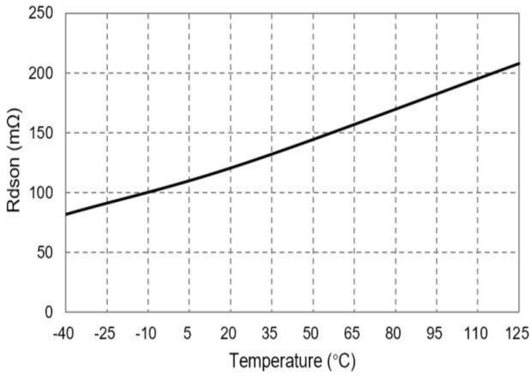
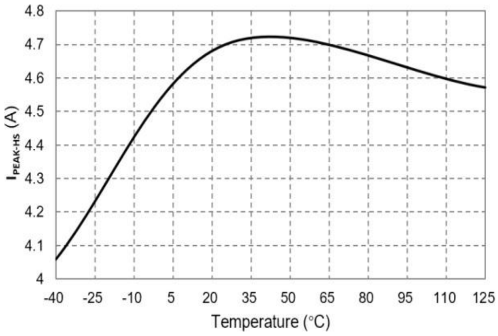
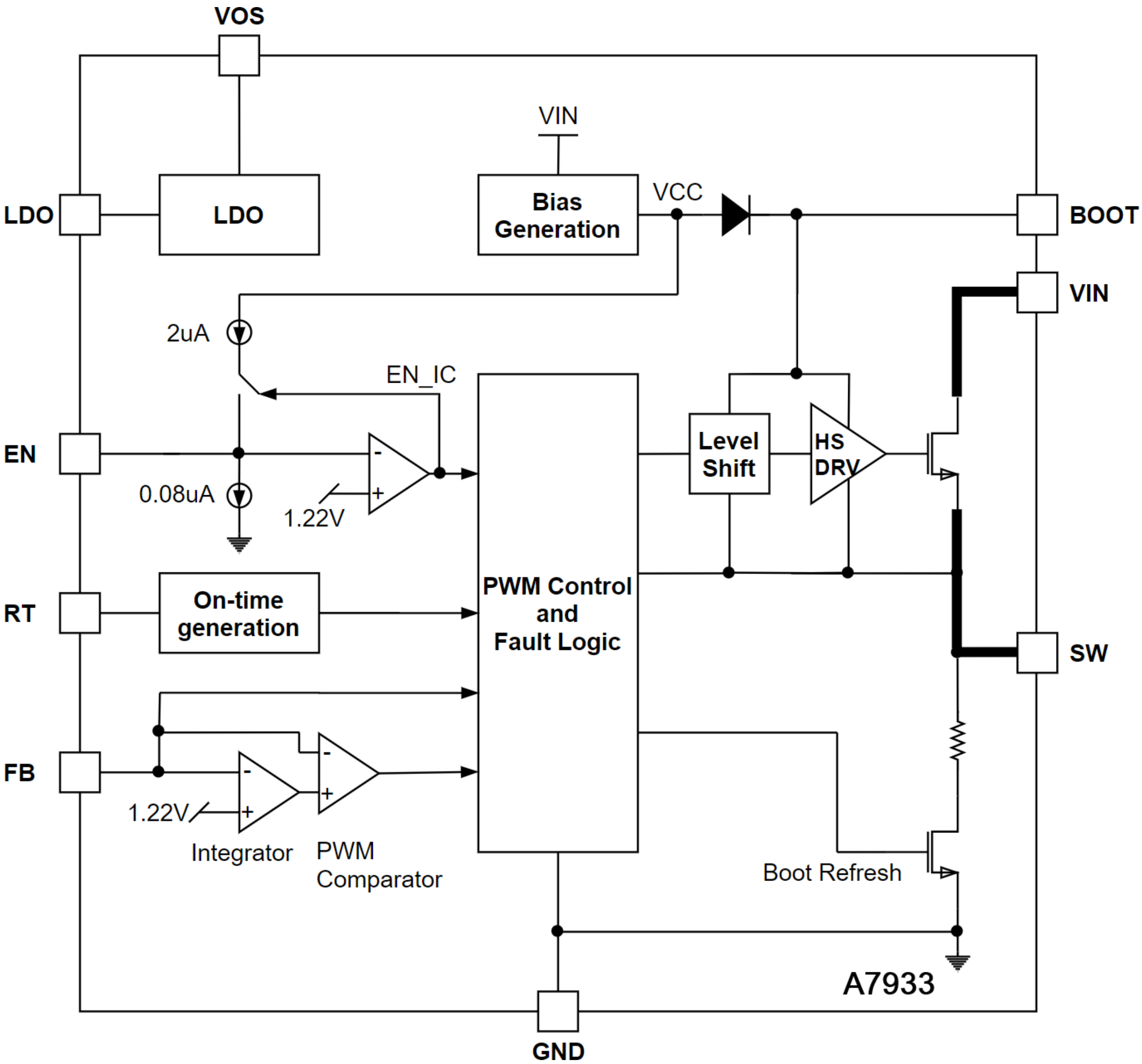


Fig 15. $I_{PEAK-HS}$ vs Temperature



BLOCK DIAGRAM



DETAILED INFORMATION

Overview

The A7933 functions within a broad input voltage range of 6.0V to 90V. Featuring an integrated main MOSFET, it can provide an output current of up to 3.2A. The A7933 utilizes constant on-time (COT) control architecture, ensuring outstanding transient response. Additionally, it includes a fixed output LDO capable of delivering up to 50mA of output current. With its patented standby circuits, the device achieves ultra-low quiescent current (IQ) and can quickly exit standby mode.

Switching Frequency (RT)

The switching frequency of the A7933 is determined by the on-time resistor on RT pin. As illustrated in Fig16, using a 110kΩ resistor establishes a switching frequency of 200kHz. It's important to note that the final switching frequency is influenced not only by component tolerances but also by $t_{ON\text{-}MIN}$ and t_{OFF}.

The formula is $F_{SW}(kHZ) = \frac{22x\,10^3}{RT(k\Omega)}$

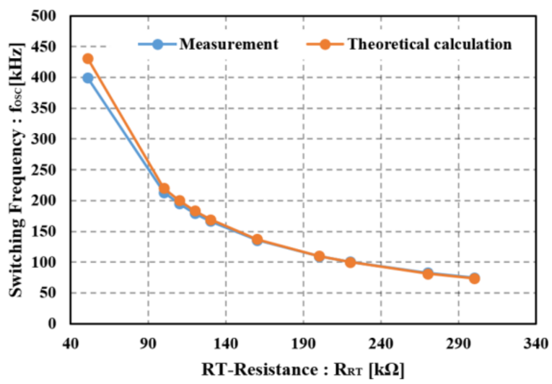


Fig16. Switching Frequency vs RT-Resistance

Output Voltage Program

Choose R_{f1} and R_{f2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{f1} and R_{f2} using below equation:

$$V_{OUT} = 1.22V \times \left(1 + \frac{R_{f1}}{R_{f2}}\right)$$

For most applications, it is recommended to use a feedback resistor (Rf1) between 100kΩ and 500kΩ. Larger feedback resistors consume less DC power, which is important for maintaining efficiency at low loads. However, using excessively large resistors is not advisable, as they can increase the susceptibility of the feedback path. Additionally, incorporating a feedforward capacitor (Cff) and a feedforward resistor (Rff) is highly recommended, as they can enhance system stability and improve transient responses. draw less DC, which is crucial for maintaining efficiency at light loads. However, excessively large resistors are not recommended as they can reduce system stability and improve transient responses.

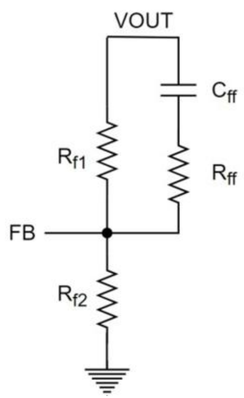


Fig.17 Feedback Resistance

Input Capacitor (CIN)

An input capacitor is essential for reducing the input ripple voltage and supplying AC current to the buck converter during each switching cycle. The input ripple voltage, ΔVIN, across the input capacitor is calculated as follows:

$$\Delta V_{IN} = \frac{I_{OuT} \text{ x } D \text{ x } (1-D)}{F_{sw} \text{ x } C_{IN}} + I_{OuT} \text{ x } R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geqq \frac{I_{OuT} \text{ x } D \text{ x } (1-D)}{F_{sw} \text{ x } (\Delta V_{IN} - I_{OuT} \text{ x } R_{ESR})}$$

To reduce the potential noise issue, it is advisable to use a capacitor rated X5R or higher with an appropriate voltage rating. This capacitor should be positioned near the VIN and GND pins to minimize the loop area created by the CIN and the VIN/GND connections. For this application, a 1μF low ESR ceramic capacitor is recommended.

Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current I_{OUT}(max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OuT}}{F_{sw} \text{ x } \Delta V_{IL}} \text{ x } \left(1 - \frac{V_{OuT}}{V_{IN}}\right)$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OuT}(\max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor should exceed the peak inductor current (IL(peak)). It is advisable to select an inductor with a saturation current that is higher than the current limit set for the A7933. Keep in mind that the saturation current levels of inductors typically decrease as the temperature rises.

Output Capacitor (COUT)

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \text{ x } F_{sw} \text{ x } C_{OUT}}$$

The equation above only accounts for the steady-state ripple. It's also important to consider transient requirements when choosing the output capacitor. A ceramic capacitor rated X5R or higher, with a capacitance greater than 22μF, is recommended. Additionally, for applications with high peak currents, an electrolytic capacitor larger than 100μF is also advised.

Enable Operation

Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}})\ x\ V_{ENH}$$

V_{ENH} is EN rising threshold voltage, typical is 1.24V.

The UVLO hysteresis is achieved using an internal 2μA current source that is turned on or off within the impedance of the set-point divider. When the voltage at the EN pin surpasses the rising threshold, the current source activates, rapidly increasing the voltage at the EN pin. The hysteresis can be calculated as follows:

$$V_{hys}(V) = R_{EN1}\ x\ 2\mu A$$

Tie EN pin to V_{IN} if hysteresis function is not used to improve quiescent current.

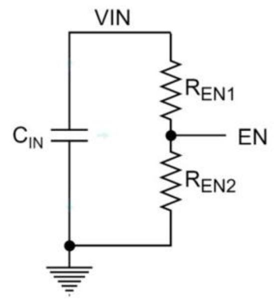


Fig 18. Enable Resistance Divider

Boot-strap capacitor

This capacitor supplies energy to the high-side gate driver. It is recommended to use a high-quality 0.1uF ceramic capacitor between the BOOT pin and the SW pin. Additionally, an RC series network can be employed to reduce the turn-on speed of the high-side MOSFET.

Catch diode

To connect an external catch diode between the SW pin and the GND pin of the A7933. Ensure that the diode meets the absolute maximum ratings for the application. The reverse voltage rating should exceed the maximum voltage of the VIN pin. Additionally, select a diode with a saturation current greater than the sum of the maximum output current and half of the inductor ripple current (ΔIL). For improved efficiency and thermal performance, opt for a catch diode with a lower voltage drop, such as the SM540C~SM5100C.

LDO

The A7933 features a 3.3V/50mA low-dropout regulator (LDO) that is ideal for powering the MCU's bias input. This LDO converts VOS to 3.3V and can deliver up to 50mA. For optimal performance, a ceramic capacitor greater than 1μF should be placed as close as possible to the LDO pin in the application.

APPLICATION AND IMPLEMENTATION

Reference Design1

Parameter	Symbol	Specification Value
Input Voltage	VIN	24V ~ 90V
Output Voltage	VOUT	5.0V
Switching Frequency	F_{SW}	200kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	3A

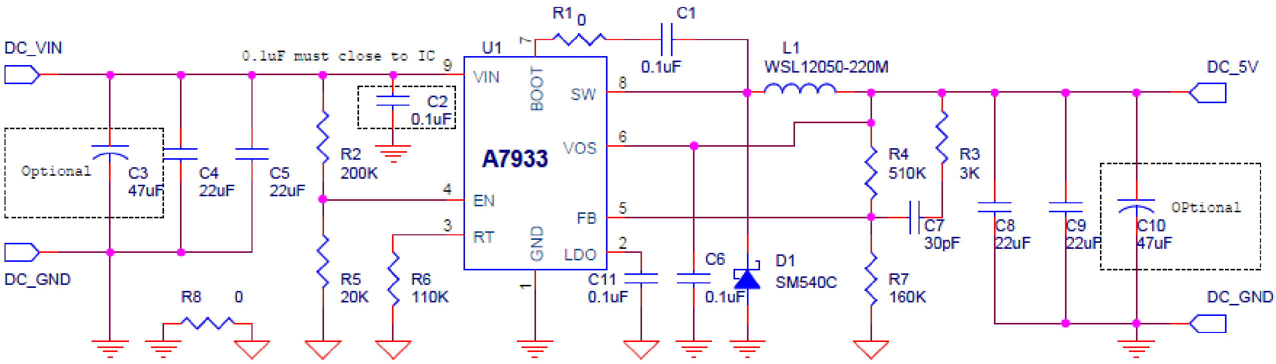


Fig 19. VOUT=5V Schematic

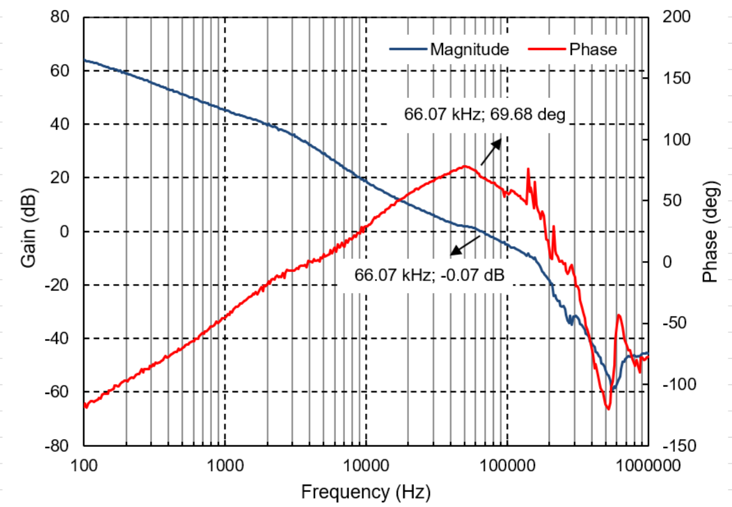


Fig 20. Frequency Characteristics (IOUT = 3.0A, VOUT=5V)

Reference Design2

Parameter	Symbol	Specification Value
Input Voltage	VIN	24V~ 75V
Output Voltage	VOUT	12V
Switching Frequency	F_{SW}	200kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	3A

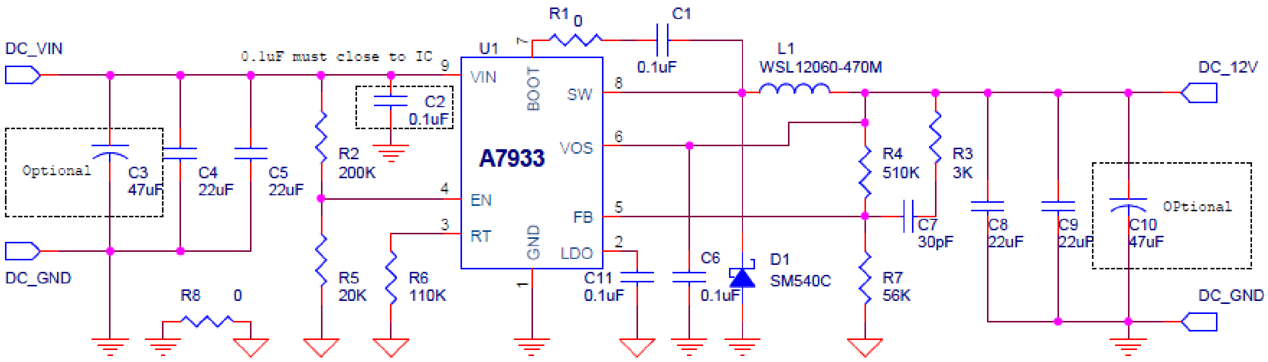


Fig 21. VOUT=12V Schematic

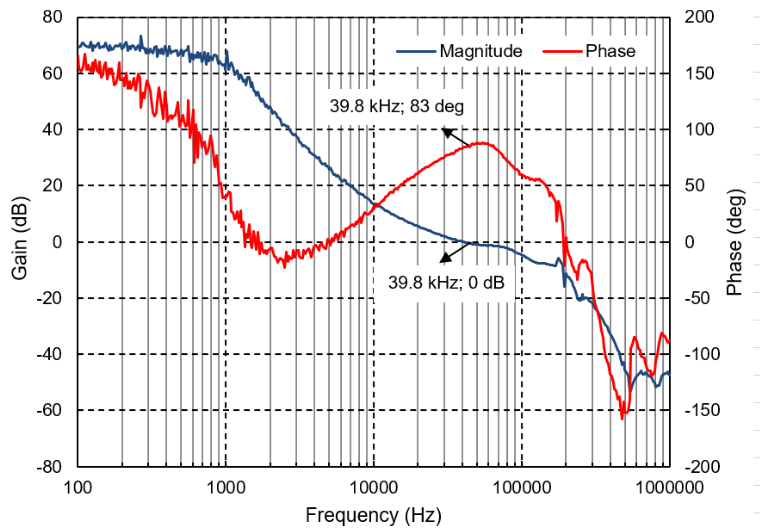


Fig 22. Frequency Characteristics (IOUT = 3.0A, VOUT=12V)

Reference Design3

Parameter	Symbol	Specification Value
Input Voltage	VIN	35V~ 75V
Output Voltage	VOUT	24V
Switching Frequency	f_{OSC}	200kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	3A

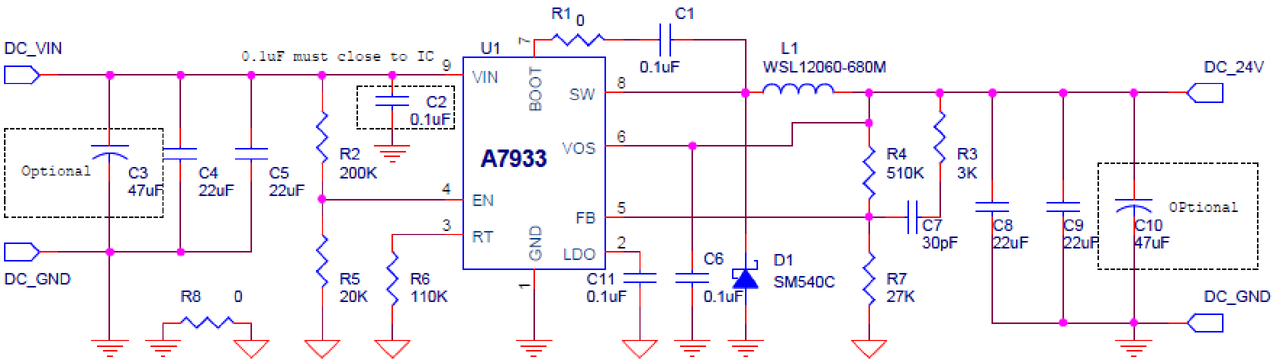


Fig 23. VOUT=24V Schematic

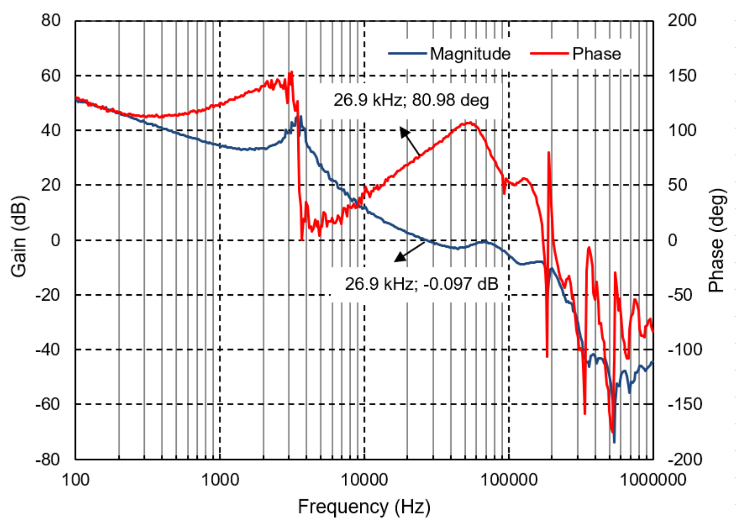


Fig 24. Frequency Characteristics (IOUT = 3.0 A, VOUT=24V)

LAYOUT GUIDELINES

To ensure optimal performance of the A7933, adhere to the following layout guidelines:

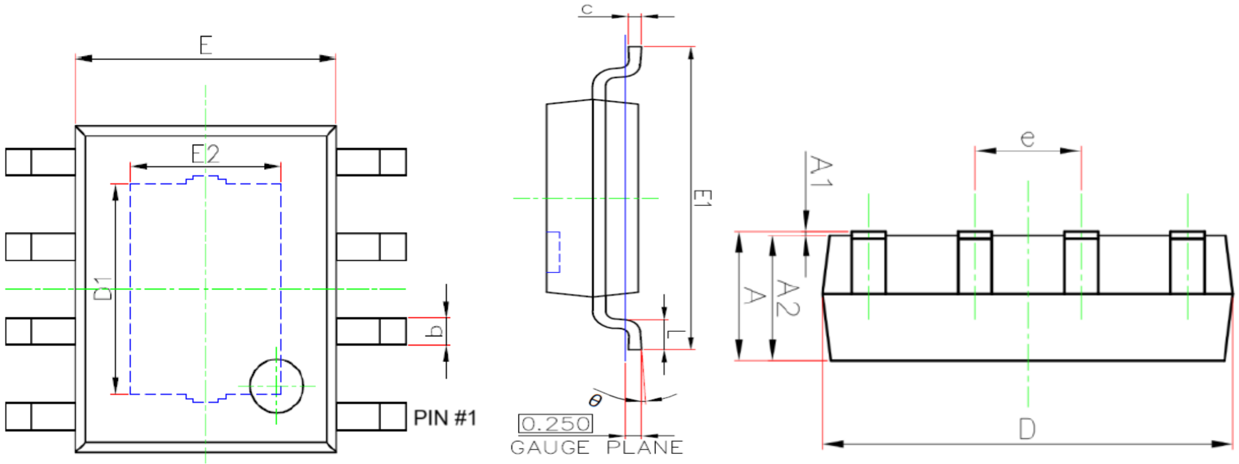
1. Use at least one low-ESR ceramic bypass capacitor (CIN). Position the CIN as close as possible to the VIN and GND pins of the A7933, and place decoupling capacitors as near as possible between the VIN and the GND of the catch diode.

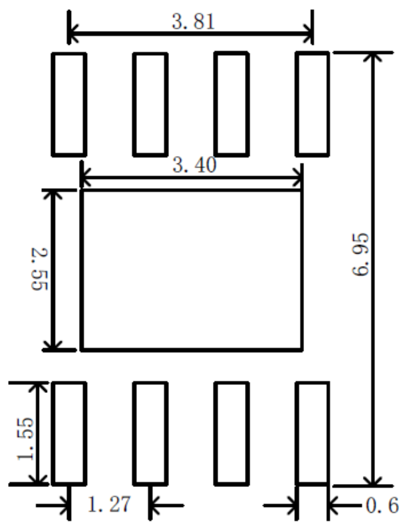
2. Reduce the loop area created by the connections of CIN to the VIN and GND pins.

3. Position the inductor close to the SW pin and minimize the area of the SW trace to prevent potential noise issues.
4. Optimize the PCB area around the VIN pin and thermal pad. If possible, incorporate a ground plane to serve as both noise shielding and a heat dissipation pathway.
5. Position the feedback resistors, Rf1 and Rf2, near the FB pin. Ensure that the feedback VOUT sensing path is routed away from noisy areas, such as the SW net.
6. Connect the VOS pin directly to the output capacitor, and place a 0.1μF capacitor between VOS and GND.
7. The RT pin is susceptible to noise, so the resistor for setting the on-time (RT) should be located close to the device.

PACKAGE INFORMATION

Dimension in PSOP8 (Unit:mm)





Symbol	Millimeters	
	Min	Max
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
D1	3.050	3.250
E2	2.160	2.360
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

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