DESCRIPTION

The AL165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (SER), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input ($\overline{PL}$) is Low the data from D0 to D7 is loaded into the shift register asynchronously.

When $\overline{PL}$ is High data enters the register serially at SER. When the clock enable input ($\overline{CE}$) is Low data is shifted on the Low-to-High transitions of the CLK input. A High on $\overline{CE}$ will disable the CLK input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in High-to-Low level shifting applications.

The AL165 is available in SOP16 and TSSOP16 packages.

ORDERING INFORMATION

Package Type	Part Number	
SOP16 SPQ: 4,000/Reel	M16	AL165M16R
		AL165M16VR
TSSOP16 SPQ: 4,000/Reel	TMX16	AL165TMX16R
		AL165TMX16VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

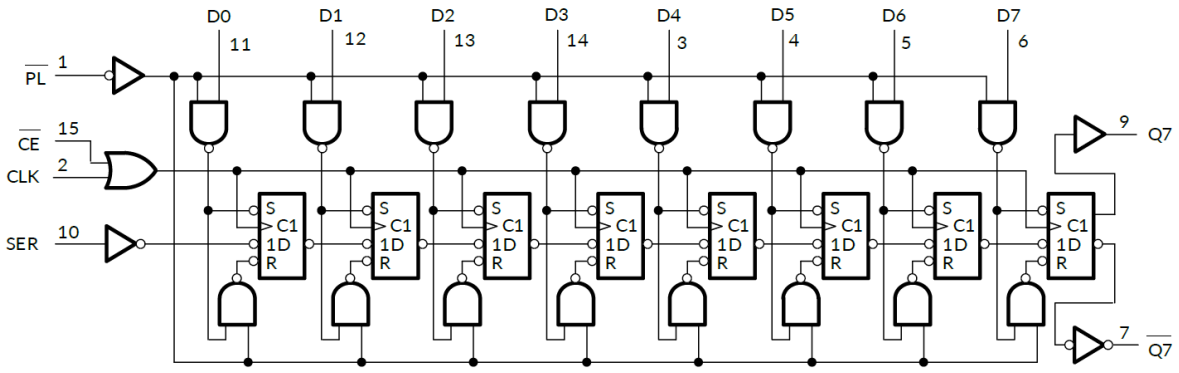
FEATURES

- 8-bit parallel-in, serial-out shift
- Power-Supply Range: 1.65V to 5.5V
- High-current output drive ±10mA @ 5V
- Low Power Consumption: 8μA(Max.)
- Low Input Current: 1μA(Max.)
- Gated Serial Data Input
- Asynchronous Master Reset
- Extended Temperature: -40°C to +125°C

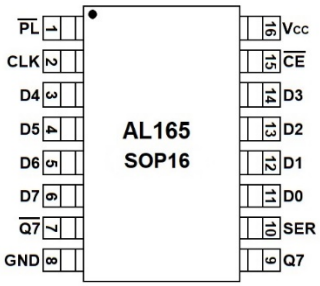
APPLICATION

- Video Display Systems
- Programable Logic Controllers
- Enterprise and Communications
- Industrial
- Appliances
- LED Displays
- Output Expander

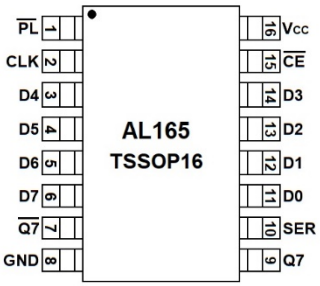
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION



SOP16, M16
Top View



TSSOP16, TMX16
Top View

Pin #		Symbol	I/O*	Function
SOP16	TSSOP16			
1	1	$\overline{PL}$	-	Asynchronous parallel load input (active Low)
2	2	CLK	I	Clock input (Low-to-High, edge-triggered)
3	3	D4	O	Parallel data inputs
4	4	D5	O	Parallel data inputs
5	5	D6	O	Parallel data inputs
6	6	D7	O	Parallel data inputs
7	7	$\overline{Q7}$	O	Complementary output from the last stage
8	8	GND	G	Ground.
9	9	Q7	O	Serial output from the last stage
10	10	SER	I	Serial data input
11	11	D0	O	Parallel data inputs
12	12	D1	O	Parallel data inputs
13	13	D2	O	Parallel data inputs
14	14	D3	O	Parallel data inputs
15	15	$\overline{CE}$	I	Clock enable input (active Low)
16	16	V_{CC}	P	Supply voltage

*I=Input, O=Output, P=Power, G=Ground.

FUNCTION TABLE

Operating Modes	Input					Qn Register		Output	
	$\overline{PL}$	$\overline{CE}$	CLK	SER	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial Shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
Hold "Do Nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

H = High voltage level; h = High voltage level one set-up time prior to the Low-to-High clock transition;
L = Low voltage level; l = Low voltage level one set-up time prior to the Low-to-High clock transition;
q = Lower case letters indicate the state of the referenced input one set-up time prior to the Low-to-High clock transition;
↑ = Low-to-High clock transition; X = don't care

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

V_{CC}, Supply Voltage Range		-0.5V~+6.5V
I_{IK}, Input Clamp Current	V_I < -0.5V or V_I > V_{CC} + 0.5V	±20mA
I_{OK}, Output Clamp Current	V_O < -0.4V or V_O > V_{CC} +0.4V	±20mA
I_O, Output Current	-0.5V < V_O < V_{CC} +0.5V	±25mA
I_{CC}, Supply Current		+50mA
I_{GND}, Ground Current		-50mA
θ_{JA}, Package Thermal Impedance (1)	SOP16	150℃/W
	TSSOP16	45℃/W
T_J, Junction Temperature (2)		-40℃ ~ +150℃
T_{STG}, Storage Temperature		-65℃ ~ +150℃
ESD Ratings		
$V_{(ESD)}$, Electrostatic Discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000V
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000V
	Machine Model (MM), JESD22-A115C (2010)	±200V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The package thermal impedance is calculated in accordance with JESD-51.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		1.65	-	5.5	V
Input Voltage	V_I		0	-	V_{CC}	V
Output Voltage	V_O		0	-	V_{CC}	V
Input Transition Rise or Fall Rate(Δt/Δv)	Data inputs	V_{CC}=1.65V to 1.95V	-	-	20	ns/V
		V_{CC}=2.3V to 2.7V	-	-	20	
		V_{CC}=3V to 3.6V	-	-	10	
		V_{CC}=4.5V to 5.5V	-	-	5	
Operating Temperature	T_A		-40	-	125	℃

SWITCHING CHARACTERISTICS

.

Parameter		-40°C to +125°C (Typ. @25°C)												Unit
		V_{CC}=1.8V±0.15V			V_{CC}=2.5V±0.2V			V_{CC}=3.3V±0.3V			V_{CC}=5V±0.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{pd}	Propagation Delay CLK or $\overline{CE}$ to Q7 or $\overline{Q7}$ (1)	-	44	-	-	20	-	-	14	-	-	9	-	ns
	Propagation Delay D7 to Q7 or $\overline{Q7}$	-	29	-	-	17	-	-	12	-	-	9	-	ns
	Propagation Delay $\overline{PL}$ to Q7 or $\overline{Q7}$	-	32	-	-	17	-	-	12	-	-	8	-	ns
t_t	Transition Time Q7 or $\overline{Q7}$ Output (2)	-	19	-	-	10	-	-	8	-	-	6	-	ns
t_w	Pulse Width	-	30	-	-	25	-	-	20	-	-	20	-	ns
t_h	Hold Width SER to CLK or $\overline{CE}$	-	-12	-	-	-5	-	-	-5	-	-	-3	-	ns
	Hold Width Dn to $\overline{PL}$	-	-5	-	-	-5	-	-	-1.5	-	-	-1	-	ns
t_{SU}	Set-Up Time SER to CLK or $\overline{CE}$	-	11	-	-	5	-	-	5	-	-	3	-	ns
	Set-Up Time Dn to $\overline{PL}$	-	5	-	-	5	-	-	1.5	-	-	1	-	ns
t_{REC}	Recovery Time $\overline{PL}$ to CLK or $\overline{CE}$	-	5	-	-	1.5	-	-	1	-	-	1	-	ns
f_{max}	Maximum Frequency For CLK C_L=15pF	-	4	-	-	10	-	-	20	-	-	30	-	MHz

(1) t_{pd} is the same as t_{PHL} and t_{PLH}. (2) t_t is the same as t_{THL} and t_{TLH}.

OPERATING CHARACTERISTICS

T_A=25°C

Parameter	Test Conditions	V_{CC}=3.3V	V_{CC}=5V	Unit
		Typ.	Typ.	
C_{pd} *	C_L=0, f=10MHz	11	17	pF

***** Power dissipation capacitance per transceiver.

ELECTRICAL CHARACTERISTICS

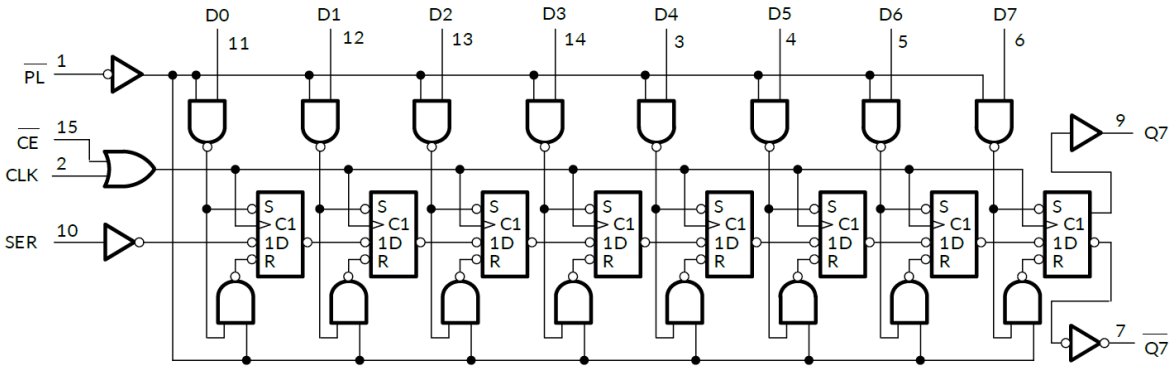
Over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	V_{CC}	TEMP	Min. (1)	Typ. (2)	Max. (1)	Unit
V_{IH}	High-Level Input Voltage		1.65V to 1.95V	+25°C	0.65x V_{CCI}	-	-	V
			2.3V to 2.7V		1.7	-	-	
			3V to 3.6V		2.0	-	-	
			4.5V to 5.5V		0.70x V_{CCI}	-	-	
V_{IL}	Low-Level Input Voltage		1.65V to 1.95V	+25°C	-	-	0.35x V_{CCI}	V
			2.3V to 2.7V		-	-	0.7	
			3V to 3.6V		-	-	0.8	
			4.5V to 5.5V		-	-	0.30x V_{CCI}	
V_{OH}	High-Level Output Voltage	I_{OH} = -100μA	1.65V to 5.5V	+25°C	V_{CC}-0.1	-	-	V
		I_{OH} = -4mA	3V		1.2	-	-	
		I_{OH} = -8mA	3.3V		1.9	-	-	
		I_{OH} = -10mA	5.0V		3.8	-	-	
V_{OL}	Low-Level Output Voltage	I_{OL} = 100μA	1.65V to 5.5V	+25°C	-	-	0.10	V
		I_{OL} = 4mA	3V		-	-	0.45	
		I_{OL} = 8mA	3.3V		-	-	0.30	
		I_{OL} = 10mA	5.0V		-	-	0.40	
I_I	Input Leakage Current	V_I=5.5V or GND	0V to 5.5V	+25°C	-	±0.1	±1	μA
				-40°C to +125°C	-	-	±5	
I_{off}		V_I or V_O=5.5V	0	+25°C	-	±0.1	±1	μA
				-40°C to +125°C	-	-	±10	
I_{CC}	Supply Current	V_I=5.5V or GND; I_O=0	1.65V to 5.5V	+25°C	-	0.1	8	μA
				-40°C to +125°C	-	-	160	
ΔI_{CC}		One Input at V_{CC}-0.6V, Other Inputs at V_{CC} or GND	3V to 5.5V	-40°C to +125°C	-	-	500	μA
C_I	Input Capacitance	f=1MHz	3.3V	+25°C	-	3.7	-	pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

BLOCK DIAGRAM



DETAILED INFORMATION

Parameter Measurement Information

Fig 1. The clock (CLK) or clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

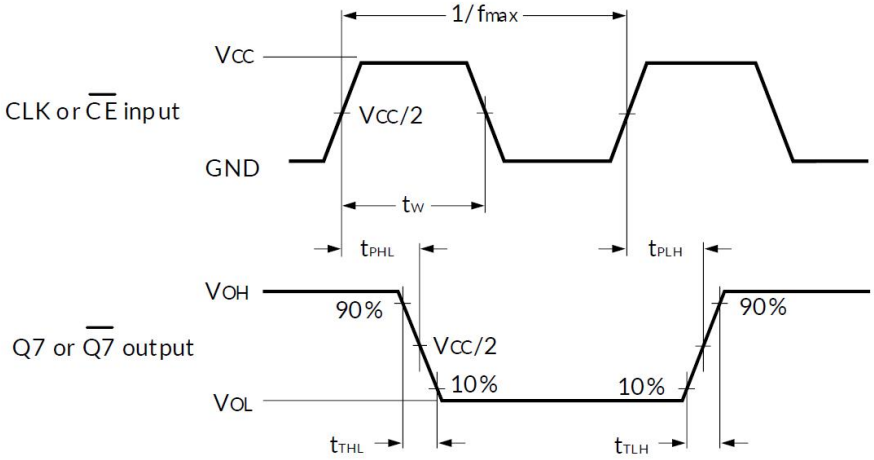


Fig 2. The parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CLK) and clock enable ($\overline{CE}$) recovery time

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

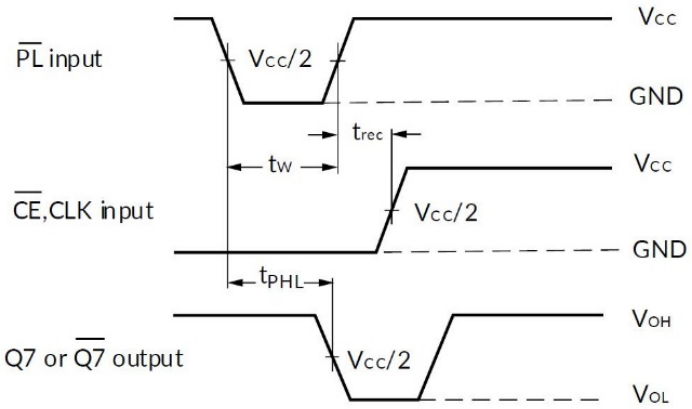


Fig 3. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

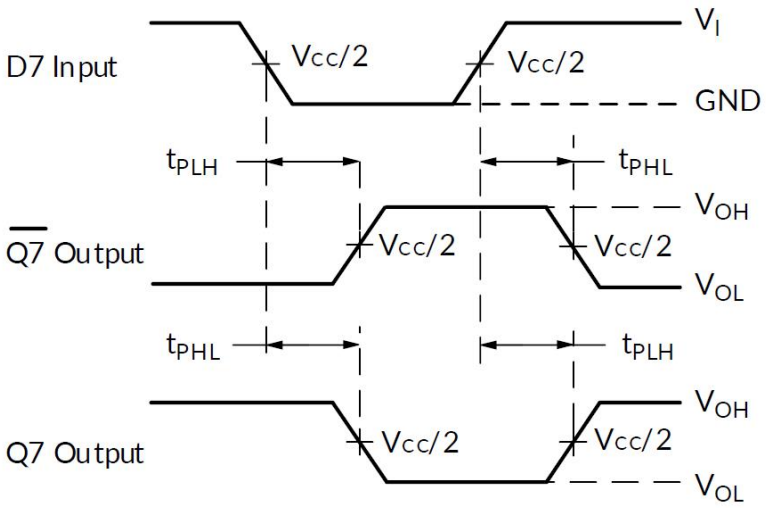


Fig 4. The set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

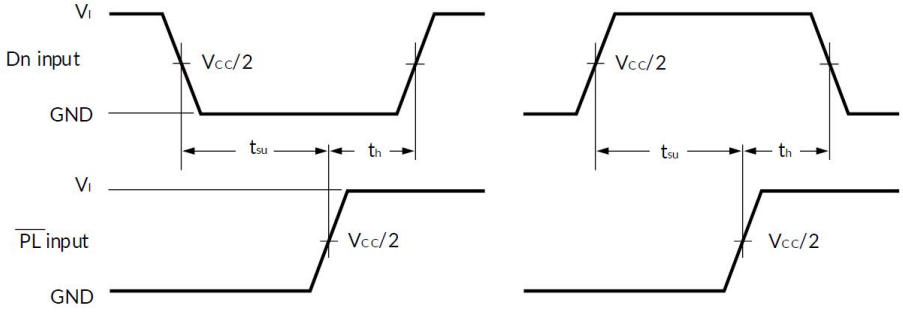


Fig 5. The set-up and hold times from the serial data input (DS) to the clock (CLK) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CLK) and from the clock input (CLK) to the clock enable input ($\overline{CE}$)

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) $\overline{CE}$ may change only from HIGH-to-LOW while CLK is LOW, see Section 1.

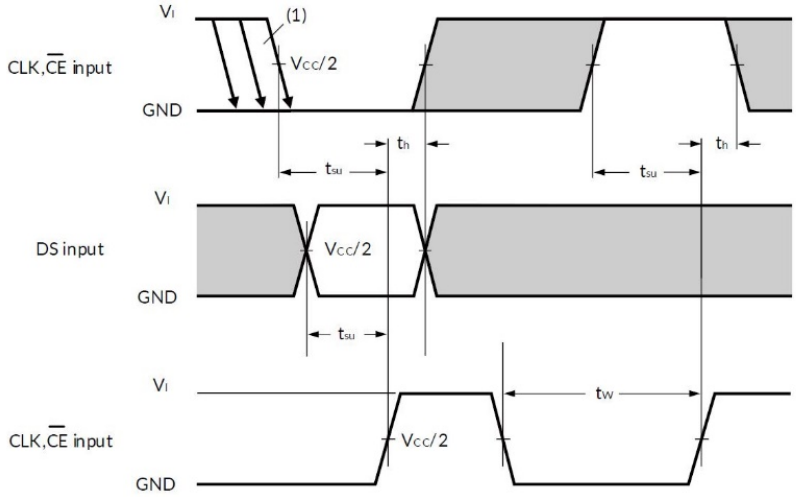


Fig 6. Test circuit for measuring switching times

Test data is given in Table 1.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Zo of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

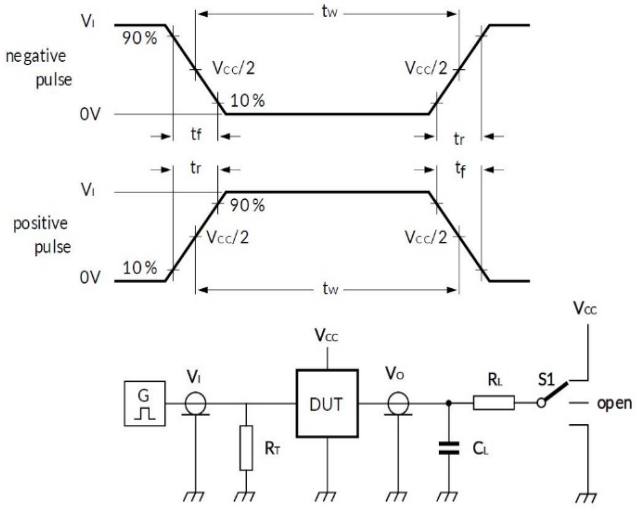
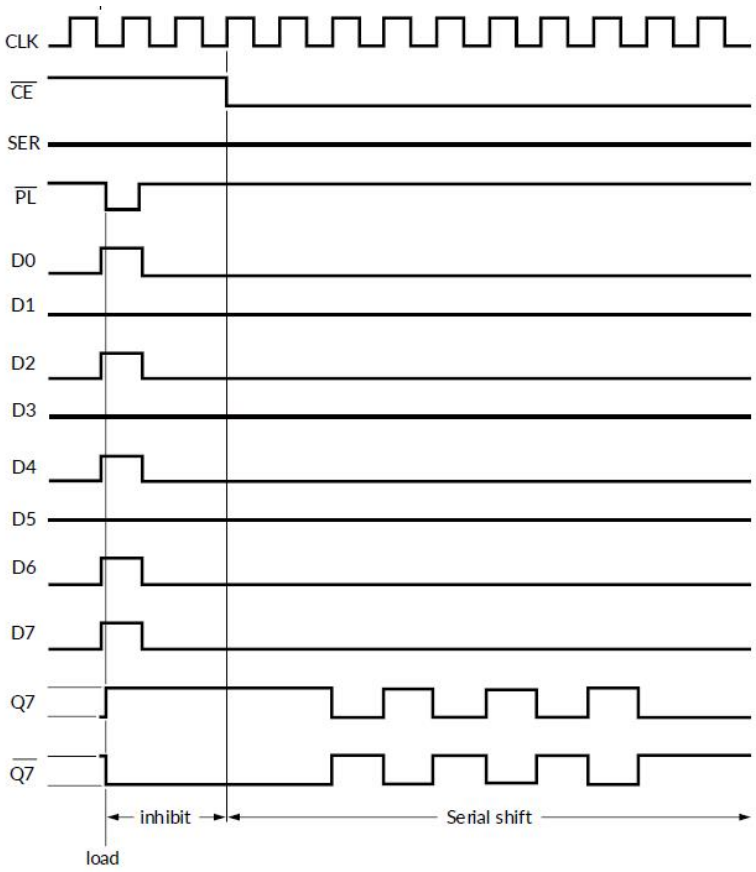


Table 1

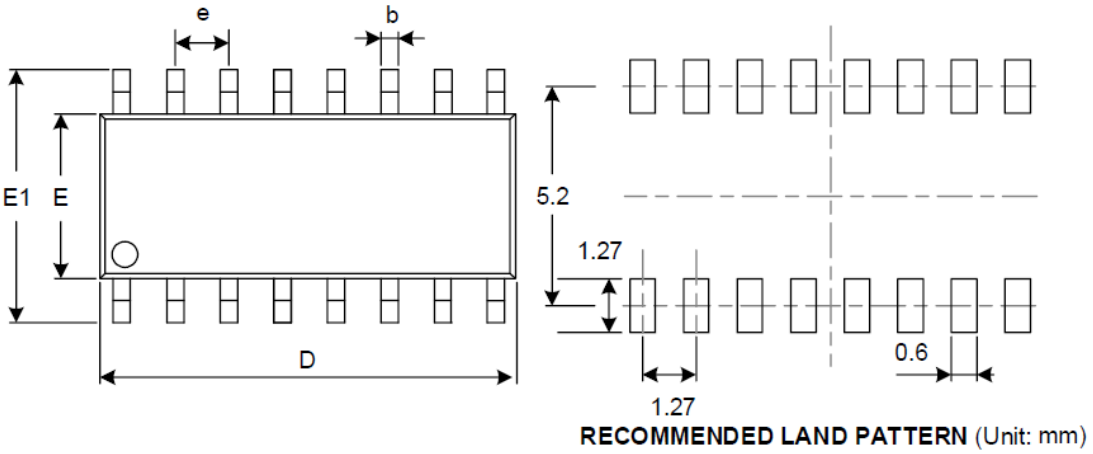
S1 position	Input		Load	
t_{PHL}/t_{PLH}	V_I	t_r, t_f	C_L	R_L
Open	V_{CC}	6ns	15pF, 50pF	1kΩ

Timing Diagram

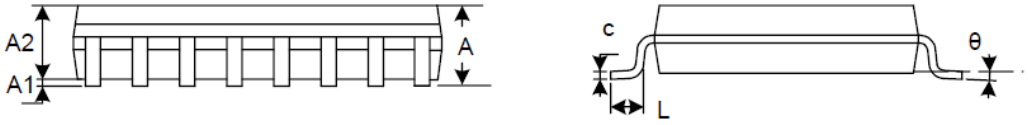


PACKAGE INFORMATION

Dimension in SOP16 (Unit: mm)

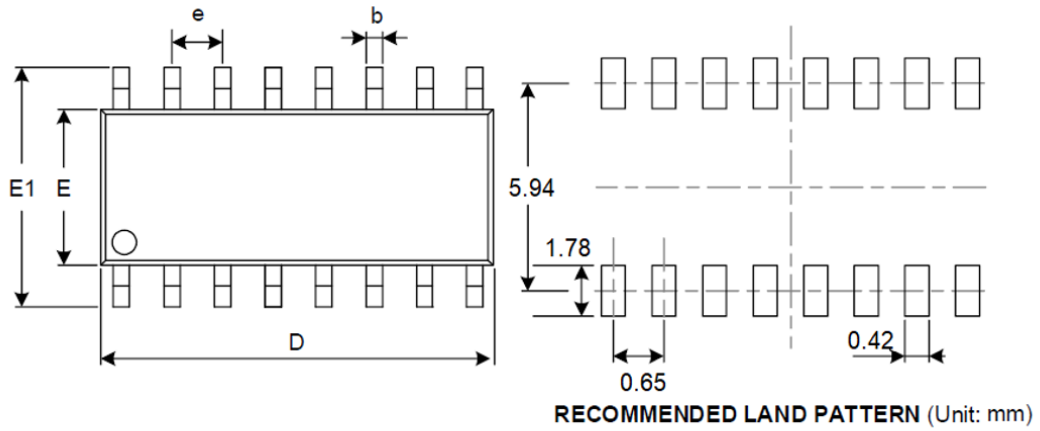


RECOMMENDED LAND PATTERN (Unit: mm)

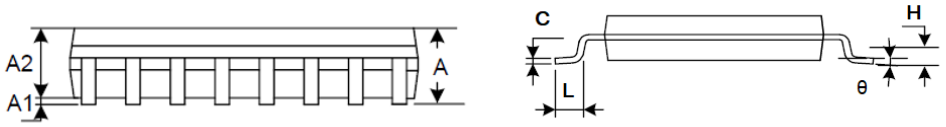


Symbol	Min.	Max.
A	-	1.750
A1	0.100	0.225
A2	1.300	1.500
b	0.390	0.470
c	0.200	0.240
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.200
e	1.270 BSC	
L	0.500	0.800
θ	0°	8°

Dimension in TSSOP16 Package (Unit: mm)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Min.	Max.
A	-	1.200
A1	0.050	0.150
A2	0.900	1.050
b	0.200	0.280
c	0.130	0.170
D	4.900	5.100
E	4.300	4.500
E1	6.200	6.600
e	0.650 BSC	
L	0.450	0.750
H	0.250 TYP	
θ	0°	8°

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