DESCRIPTION

The A4773 is an integrated power switch for self-powered and bus-powered Universal Serial Bus (USB) applications.

The A4773 is a cost-effective, low voltage, single P-channel MOSFET load switch with 70mΩ RDS(ON), which is free of parasitic body diode and has no reverse input-output leakage current. When the output voltage is higher than input voltage, the power switch is turned off by internal output reverse-voltage protector.

Several protection features include current limiting and thermal shutdown to prevent catastrophic switch failure caused by increasing power dissipation when continuous heavy loads or short circuit occurs.

FLAG is an open-drain output report over-current or over-temperature event and has typical 13ms deglitch timeout period. In addition, FLAG also reports output reverse-voltage condition with typical 5ms deglitch timeout period.

The A4773 is available in SOT-26 package.

ORDERING INFORMATION

Package Type	Part Number	
SOT-26 SPQ: 3,000psc/Reel	E6	A4773E6R
		A4773E6VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

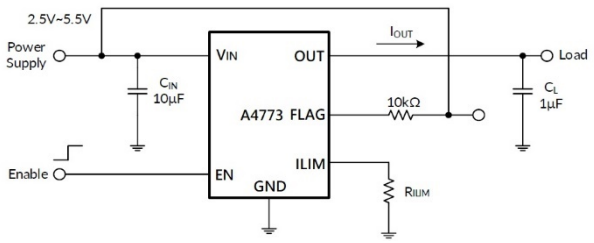
FEATURES

- Typical 27μA Low Quiescent Current
- Typical 0.1μA Shutdown Current
- No Reverse Input-Output Leakage Current
- Meets USB Current Limiting Requirements
- Adjustable Current Limit: 400mA to 2.7A
- Fast Over-Current Response
- 70mΩ High-side MOSFET
- Under Voltage Lockout
- Thermal Shutdown Protection
- Operating Range: 2.5V to 5.5V
- Built-In Soft-Start Function

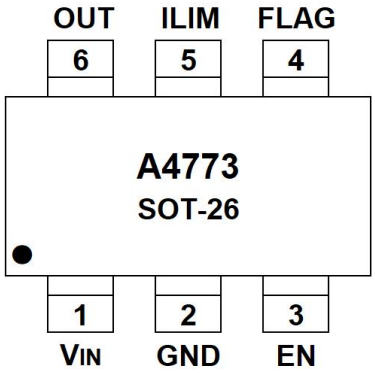
APPLICATION

- USB Host and Self-Powered Hubs
- USB Bus-Powered Hubs
- USB Power Management
- General Purpose Power Switch (High Side)
- Hot Plug-in Power Supplies
- Battery-Charger Circuits

TYPICAL APPLICATION



PIN DESCRIPTION



SOT-26, E6

Top View

SOT-26	Symbol	Function
1	V_{IN}	Power Supply Input. The P-Channel Source of Switch, Which also supplies IC's internal circuitry. Connect to Positive Supply.
2	GND	Ground.
3	EN	Enable Input. Logic Level Enable Input, Active high available. Internal pulldown.
4	FLAG	Fault Flag. Active low, open-drain output. Indicates over-current or thermal shutdown conditions. Over-current condition must last longer than td in order to assert FLAG
5	ILIM	Current limit set pin. Connect a resistor between this pin and ground to program the desired current limit set point. Do Not Float this PIN.
6	OUT	Switch Output. The P-Channel Drain of Switch, Which Typically Connects to Load.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

V_{IN}, Supply Voltage Range		-0.3V ~ +6V
V_{OUT}, Output Voltage Range		-0.3V ~ +6V
V_{EN}, EN Input Voltage		-0.3V ~ +6V
V_{ILIM}, ILIM Output Voltage		-0.3V ~ +6V
V_{FLAG}, FLAG Output Voltage		-0.3V ~ +6V
P_D, Power Dissipation		0.3W
θ_{JA}, Package Thermal Impedance (1)	SOT-26	200°C/W
T_J, Junction Temperature (2)		-40°C ~ +150°C
T_{STG}, Storage Temperature Range		-65°C ~ +150°C
T_L, Lead Temperature (Soldering,10secs)		+260°C
$V_{(ESD)}$, Electrostatic Discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±4000V
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1500V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The package thermal impedance is calculated in accordance with JESD-51.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

RECOMMENDED OPERATING CONDITIONS

Parameter	MIN	MAX	Units
V_{IN}, Supply Voltage Range	2.5	5.5	V
V_{OUT}, Output Voltage Range	0	5.5	V
V_{EN}, EN Input Voltage	0	5.5	V
V_{ILIM}, ILIM Output Voltage	0	5.5	V
I_{ILIM}, Output Current Limit	0.4	2.7	A
T_J, Junction Temperature	-40	125	℃
T_A, Operating Temperature	-40	85	℃

ELECTRICAL CHARACTERISTICS

(V_{IN}=5.0V, T_A = +25°C, unless otherwise noted.) (1)

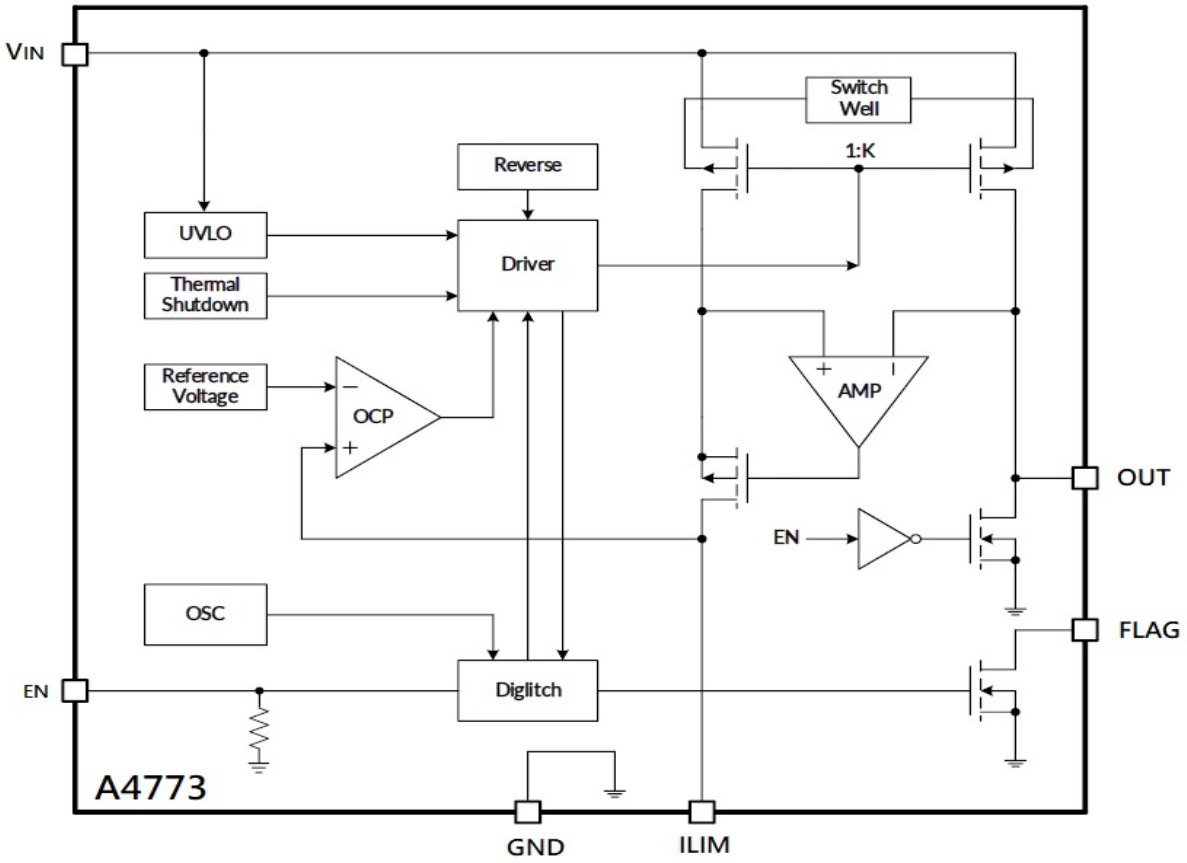
Parameter	Symbol	Conditions	Min. (2)	Typ. (3)	Max. (2)	Unit
Power Input Voltage Range	V_{IN}	-	2.5	-	5.5	V
Power Supply Current	I_Q	Switch on, V_{OUT}=Open	-	27	50	μA
Shutdown Supply Current	I_{SD}	Switch off, V_{OUT}=Open	-	0.1	1.0	μA
Under-Voltage Lockout Threshold	V_{UVLO}	C_{IN}=10μF	-	1.9	2.4	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HY}	C_{IN}=10μF	-	0.1	0.2	V
Switch Resistance	$R_{DS(ON)}$	I_{OUT}=500mA	-	70	80	mΩ
Enable Input Threshold	V_{IH}	V_{IN}=2.5V to 5.5V, C_{IN}=10μF	1.6	-	-	V
	V_{IL}		-	-	0.4	V
Enable Pull Down Resistance	R_{EN}	V_{IN}=2.5V to 5.5V	-	500	-	kΩ
Output Turn-On Delay Time	t_{ON}	C_{IN}=10μF, R_L=10Ω, C_L=1μF	-	2.0	3.0	ms
Output Turn-Off Delay Time	t_{OFF}		-	20	50	μs
Response Time to Short Circuit	t_{SCR}	C_{IN}=470μF to 1000μF	-	6.0	-	μs
Current Limit Threshold	I_{LIMIT}	C_{IN}=10μF, C_L=1μF, R_{ILIM}=27K	0.44	0.5	0.56	A
Short-Circuit Current Threshold	I_{SHORT}		-	0.375	-	A
Over-Current FLAG Response Delay Time	t_D	C_{IN}=10μF, C_L=1μF, V_{OUT}=0 until FLAG is low	-	13	20	ms
FLAG Output Low Voltage	V_{FLAG_L}	C_{IN}=10μF, I_{SINK}=2mA	-	-	0.4	V
FLAG Output Leakage Current	I_{FLAG_L}	C_{IN}=10μF, V_{OC}=5V	-	0.1	1	μA
OUT Shutdown Discharge Resistance	R_{DIS}	C_{IN}=10μF, Switch off	-	270	350	Ω
Thermal Shutdown Temperature	T_{SD}	C_{IN}=10μF	-	145	-	℃
Thermal Shutdown Hysteresis	T_{SD_HY}		-	20	-	℃

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Quiescent Current vs. Input Voltage

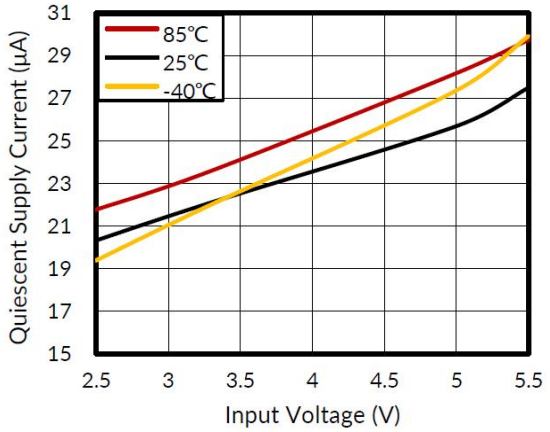


Fig.2 Shutdown Current vs. Input Voltage

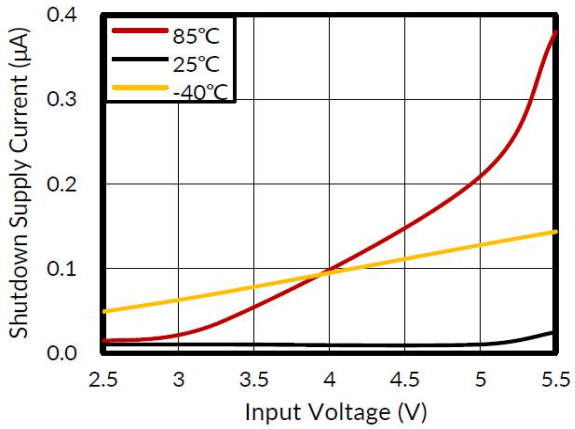


Fig.3 High-side MOSFET On Resistance vs. Input Voltage

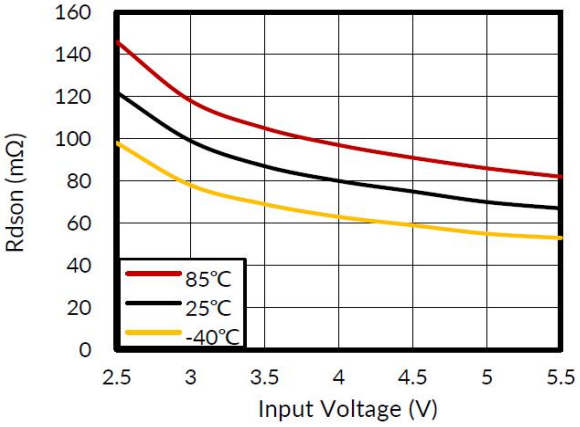


Fig.4 High-side MOSFET On Resistance vs. Temperature

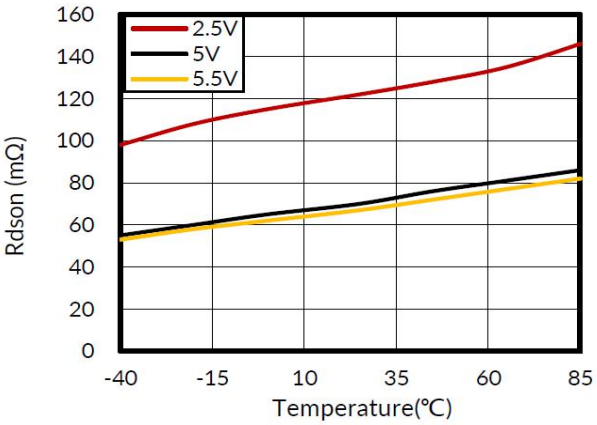


Fig.5 Current Limit Threshold vs. Input Voltage

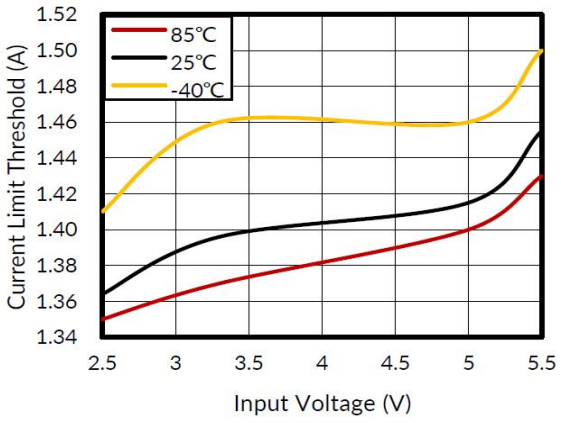


Fig.6 Current Limit Threshold vs. Temperature

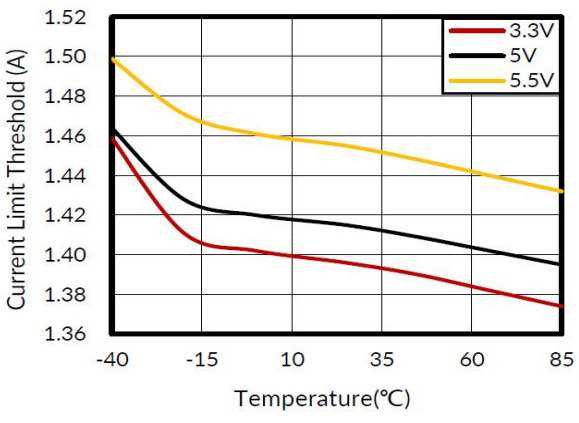


Fig.7 Enable Threshold vs. Input Voltage

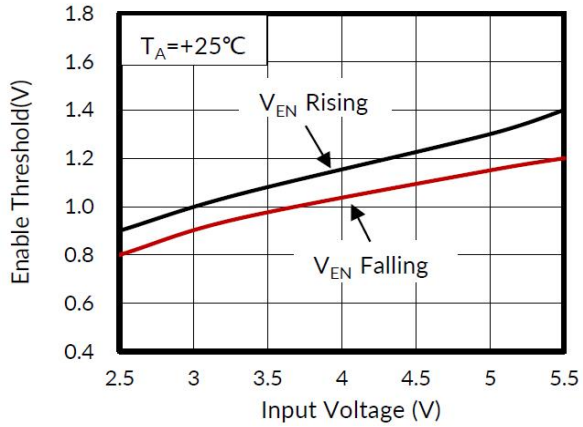


Fig.8 Enable Threshold vs. Temperature

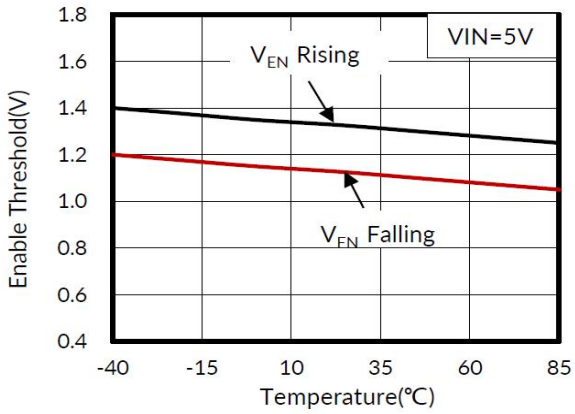


Fig.9 UVLO Threshold vs. Temperature

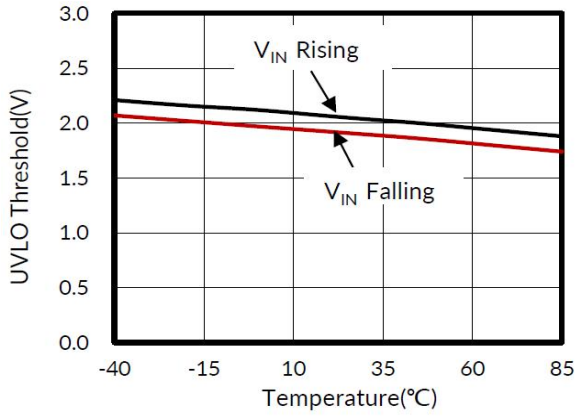


Fig.10 Current Limit Threshold vs. R_{ILIM}

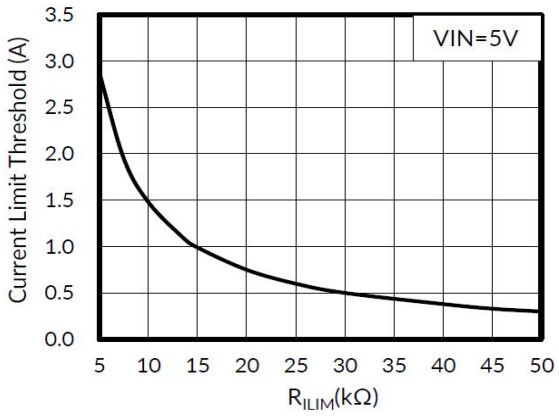


Fig.11 Turn-On Delay Time

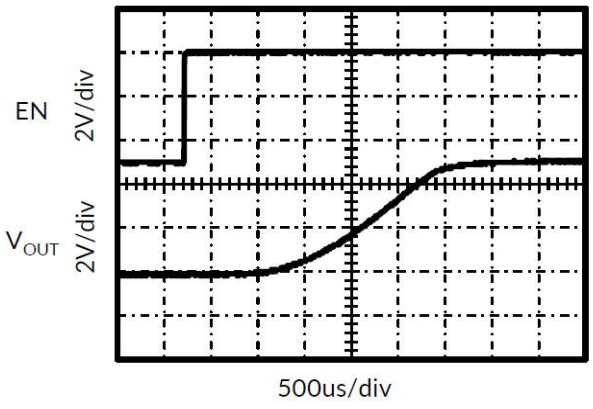


Fig.12 Turn-Off Delay Time

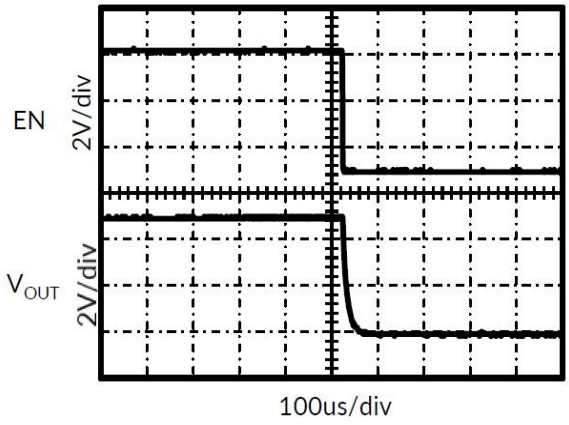


Fig.13 UVLO at V_{IN} Rising

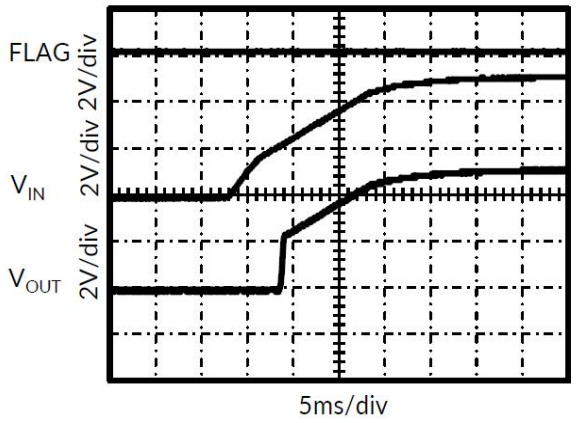


Fig.14 UVLO at V_{IN} Falling

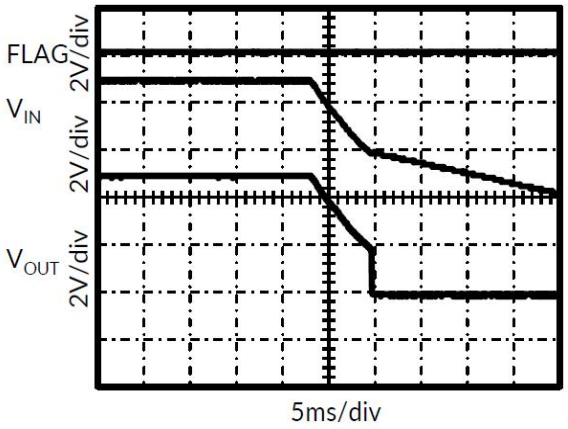


Fig.15 Exit Over Temperature Protection

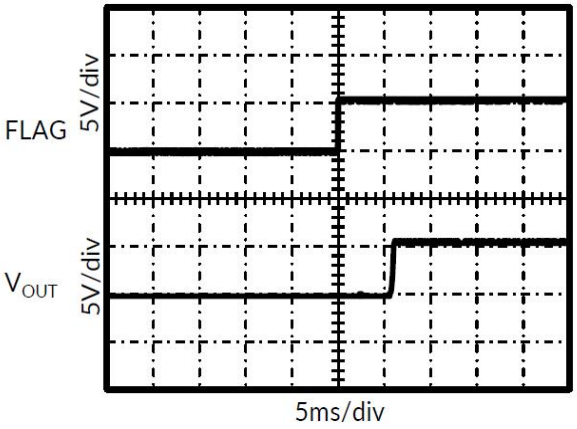


Fig.16 Enter Over Temperature Protection

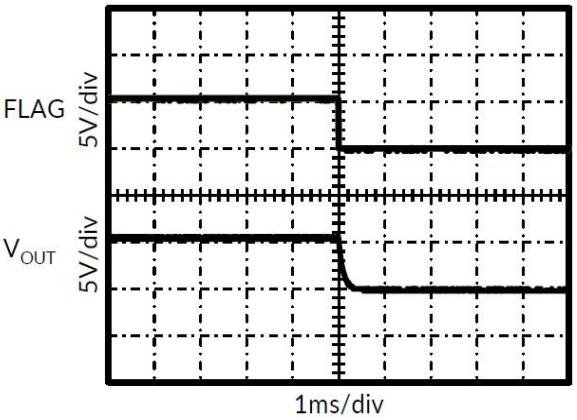


Fig.17 No Load into Short-Circuit

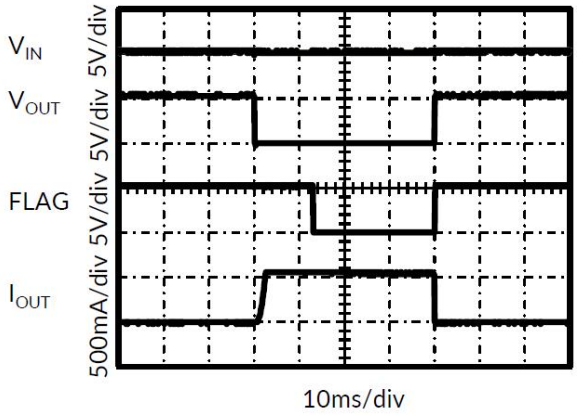


Fig.18 Device Enabled into Short-Circuit

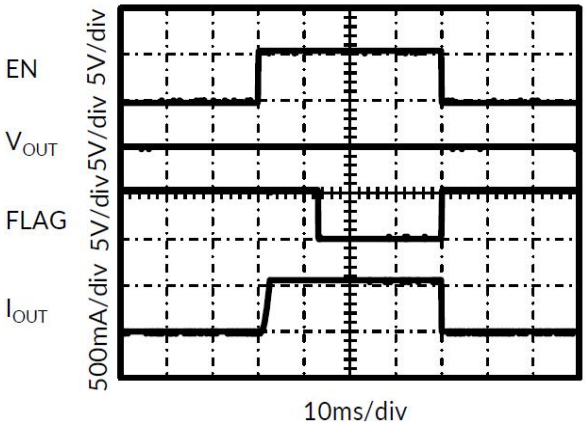
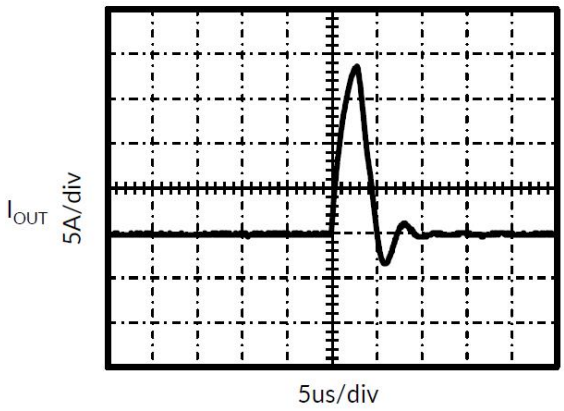


Fig.19 Short-Circuit Response Time



DETAILED INFORMATION

Parameter Measurement:

Fig.20 Switch Turn-On and Turn-Off Delay Time

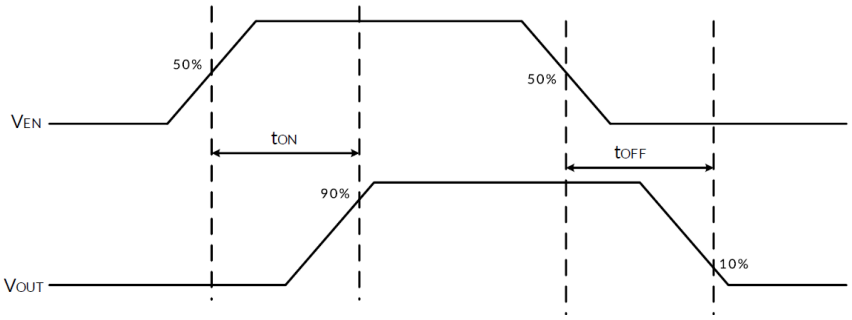
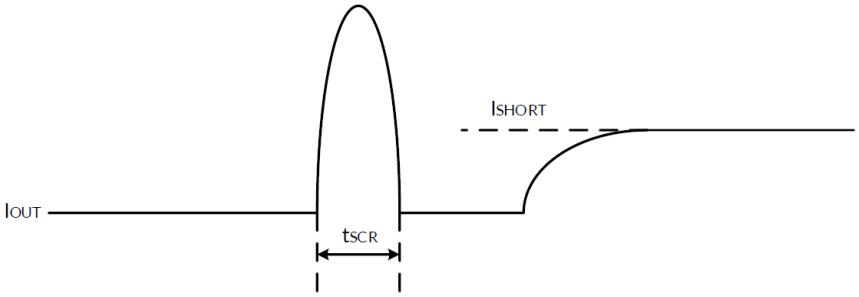


Fig.21 Short-Circuit Response Time



Input and Output

V_{IN} is the power supply connection to the logic circuitry and the source of the P-channel MOSFET. OUT is the drain of the P-channel MOSFET. In a typical circuit, current flows from V_{IN} to OUT toward the load. The output P-channel MOSFET and driver circuit are also designed to allow the MOSFET drain to be externally forced to a higher voltage than the source (V_{OUT}>V_{IN}) when the switch is disabled.

Thermal Shutdown

Thermal shutdown is employed to protect device and load from damage because of excessive power dissipation. It shuts off the output MOSFET and asserts the FLAG output, if the die temperature exceeds 145°C until the die temperature drops to 125°C.

Soft-Start

In order to eliminate the upstream voltage sag caused by the large inrush current during hot-plug events, the soft-start feature effectively isolates power supplies from such highly capacitive loads.

Under-Voltage Lockout (UVLO)

UVLO prevents the MOSFET switch from turning on until input voltage exceeds 1.9V (Typical). If input voltage drops below 1.8V (Typical), UVLO shuts off the MOSFET switch. Under-voltage detection functions only when the switch is enabled.

Current Limiting and Short-Circuit Protection

The current limit circuit is designed to limit the output current to protect the upstream power supply. Current limit threshold is programmed with a resistor from I_{LIM} to ground marked as R_{ILIM}. It can be estimated by the following equation:

$I_{LIM} \approx \frac{13500}{R_{ILIM}}$, $I_{SHORT} \approx 0.75 \times \frac{13500}{R_{ILIM}}$

We recommend the R_{ILIM} value range：5KOhm~36KOhm. For more details, please refer to Figure 10. Under output short-circuit condition; the typical current limit folded back 75%. If the A4773 keeps at overcurrent condition for a long time, the junction temperature may exceed 145°C, and over- temperature protection will shut down the output until temperature drops 125°C or limit (short-circuit) condition is removed.

ILIM(A)	R_{ILIM}(kΩ)
0.5	29.4
1.0	14.5
1.5	9.42
2.0	7.06
2.7	5.17

Table 1. Typical Design Examples

Reverse-Voltage Protection

The reverse-voltage protection feature turns off the P-MOSFET switch whenever the output voltage exceeds the input voltage by 50mV.

Fault Flag (FLAG)

The signal is an open-drain N-MOSFET output. FLAG is asserted (active low) when an over-current, short-circuit or thermal shutdown condition occurs.

In the case of an over-current condition, FLAG will be asserted only after the response delay time (t_D) has elapsed.

This ensures that FLAG is asserted only upon valid over-current condition and that erroneous error reporting is eliminated.

False over-current condition can occur during hot-plug events when a highly capacitive load is connected and causes a high transient inrush current that exceeds the current limit threshold for up to 1ms. The FLAG response delay time t_D is 13ms (Typical).

Power Dissipation

The device's junction temperature depends on several factors such as the load, PCB layout, ambient temperature, and package type. Equations that can be used to calculate power dissipation and junction temperature are found below:

$P_D = R_{DS(ON)} \times I_{OUT}^2$

To relate this to junction temperature, the following equation can be used:

$T_J = P_D \times \theta_{JA} + T_A$

Where: T_J = junction temperature, T_A = ambient temperature,θ_{JA} = the thermal resistance of the package

Supply Filter Capacitor

In order to prevent the input voltage drooping during hot-plug events, connect a ceramic capacitor (C_{IN}) from V_{IN} to GND. The CIN is positioned close to VIN and GND of the device. However, higher capacitor values could reduce the voltage sag on the input further. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds 6.0V which is the absolute maximum supply voltage even for a short duration.
If the upstream supply cable is long or the V_{IN} transient exceeds 6.0V during the V_{OUT} short, recommend adding a second filter capacitor at the upstream supply output terminal.

Output Filter Capacitor

A low-ESR 10uF ceramic capacitor between OUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1uF ceramic capacitor improves the immunity of the device to short-circuit transients.

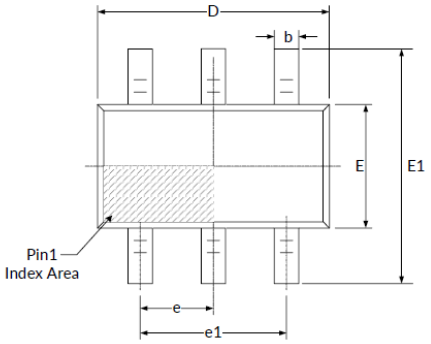
PCB Layout Guide

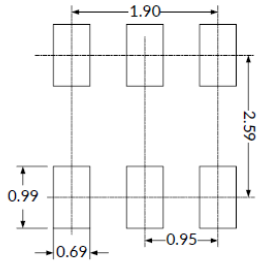
For best performance of the A4773, the following guidelines must be strictly followed:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Keep V_{IN} and OUT traces as wide and short as possible.
3. Locate A4773 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling. Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance
5. The traces routing the R_{ILIM} resistor to the A4773 should be as short as possible to reduce parasitic effects on the current limit accuracy.

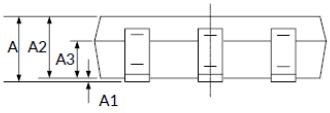
PACKAGE INFORMATION

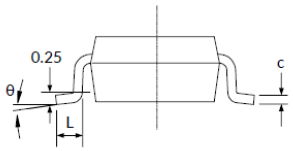
Dimension in SOT-26 Package (Unit: mm)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	MILLIMETERS	
	Min.	Max.
A	-	1.250
A1	0.020	0.110
A2	1.000	1.200
A3	0.600	0.700
b	0.330	0.410
c	0.150	0.190
D	2.800	3.000
E	1.500	1.700
E1	2.600	3.000
e	0.850	1.050
e1	1.800	2.000
L	0.350	0.550
θ	0°	8°

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