DESCRIPTION

The A6310B is a highly precise, low noise, positive voltage LDO regulators manufactured using CMOS processes. The A6310B achieves high ripple rejection and low dropout and consists of a standard voltage source, an error correction, current limiter and a phase compensation circuit plus a driver transistor. The A6310B is also compatible with low ESR ceramic capacitors which give added output stability. This stability can be maintained even during load fluctuations due to the excellent transient response of the series.

The A6310B's current limiter feedback circuit also operates as a short protect for the output current limiter.

The CE function enables the output to be turned off, resulting in greatly reduced power consumption.

The A6310B is available in PSOP8 package.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 4,000pcs/Reel	MP8	A6310BMP8
		A6310BMP8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

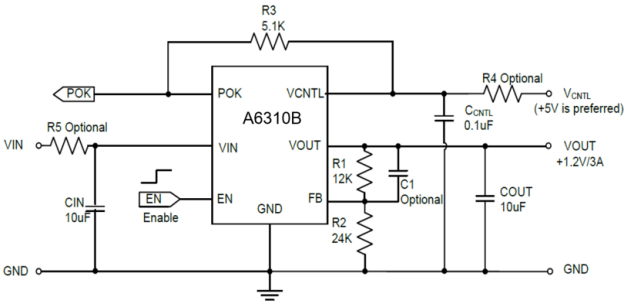
FEATURES

- Low on-resistance: 80mΩ(Typ.)
- Highly Accurate: ± 1.5%
- Dropout Voltage: 160mV @ 2A
- High Ripple Rejection: 50dB (1 kHz)
- Maximum Output Current : 3A
- Standby Current : less than 0.1μA
- Internal protector: current limiter
- Output Voltage Range: 0.8V to 5.0V

APPLICATION

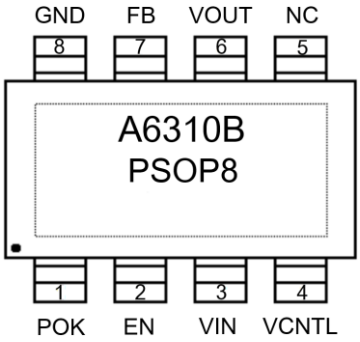
- Laptop PC
- Industrial PC
- Graphic Card

TYPICAL APPLICATION



1. Input capacitor (C_{IN}) and Output capacitor (C_{OUT}): 10.0μF or more , C_{OUT} must be less than 1000uF
2. R4 and R5 are used as input resistors to limit the surge formation of hot-swap, and should be properly selected according to the current capability requirements of the actual application

PIN DESCRIPTION



PSOP8, MP8

Top View

Pin #	Symbol	Function
1	POK	Power OK Indication
2	EN	Enable pin
3	VIN	Input Voltage
4	VCNTL	Supply Input for Control Circuit
5	NC	Not Internally Connected
6	VOUT	Output Voltage
7	FB	Feedback Voltage
8	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Input voltage	V_{CNTL}	-0.3	6.5	V
	V_{IN}	1.2	6.5	
	V_{EN}	-0.3	V_{CNTL}+0.3	
Output Voltage	V_{OUT}	-0.3	V_{IN} +0.3	
	POK	0.3	7	
	V_{FB}	-0.3	V_{CNTL}+0.3	
Power Dissipation	P_D	2.0		W
Thermal resistance	θ_{JA}	50		℃/W
Operating Ambient Temperature	T_{OPR}	-40	+125	℃
Storage Temperature	T_{STG}	-60	+150	

The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

ELECTRICAL CHARACTERISTICS

V_{CNTL}=5V, V_{IN}=1.8V, V_{OUT}=1.2V, T_A=25℃ unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Feedback Voltage	V_{FB}	I_{OUT}=30 mA	0.788	0.8	0.812	V
Dropout Voltage	V_{DROP}	V_{CNTL} =5V, V_{OUT}=1.2 I_{OUT}=2A	-	0.16	0.24	V
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{CNTL} \cdot V_{OUT}}$	3.0V ≤V_{CNTL}≤5.5V I_{OUT}=10 mA	-	0.01	0.1	%/V
Load Regulation	ΔV_{FB}	1.0 mA ≤I_{OUT} ≤3A	-	1	2	mV
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{\Delta Ta \cdot V_{OUT}}$	V_{IN}=$V_{OUT(S)}$+1.0 V, I_{OUT}=10 mA -40°C ≤ Ta ≤85°C	-	±100	-	ppm/℃
Supply Current	I_{SS1}	V_{IN}=$V_{OUT(S)}$+1.0 V , I_{OUT}=0	-	0.6	1.0	mA
Shutdown Current	I_{STB}		-	-	1	uA
FB Power OK Threshold	V_{THPOK}		-	93	-	%
POK hysteresis			-	6	-	%
Ripple-Rejection	|PSRR|	V_{IN}=$V_{OUT(S)}$+1.0 V , f=1 kHz Vrip=0.5 Vrms, I_{OUT}=50 mA	-	50	-	dB
Short-circuit Current	I_{short}	V_{OUT}=0 V	-	200	-	mA
Output Noise	e_N	I_{OUT}=30 mA,10HZ-100kHZ	-	50	-	uV_{RMS}
V_{CNTL} Undervoltage protection	V_{UVLO}		2.5	2.7	2.9	V
Hysteresis of undervoltage protection	$V_{UVLOHYS}$		-	0.3	-	V
VOUT Pull Low Resistance	-	V_{IN} = V_{CNTL} =5V,CE=0, I_{OUT}=10 mA	-	68	-	Ω
Overcurrent Protection Threshold Level	I_{lim}		2.5	3.2	-	A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL} =CE=5.0V,V_{IN}=1.8V I_{OUT}=120mA	-	170	-	℃
Thermal Shutdown Hysteresis	T_{SDHYS}	V_{CNTL} =CE=5.0V,VIN=1.8V I_{OUT}=120mA	-	50	-	℃
CE “High” Voltage	V_{CEH}		1.2	-	-	V
CE “High” Current	I_{CEH}	V_{CNTL} =V_{IN}=V_{CE}=4	-	4	-	μA

TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Dropout Voltage vs Output Current

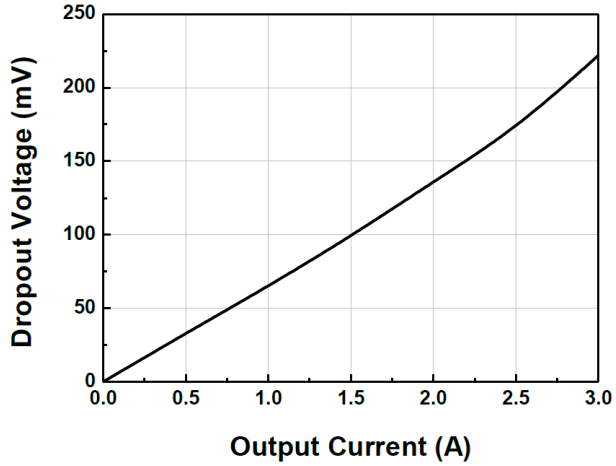


Fig.2 Output Voltage vs Temperature

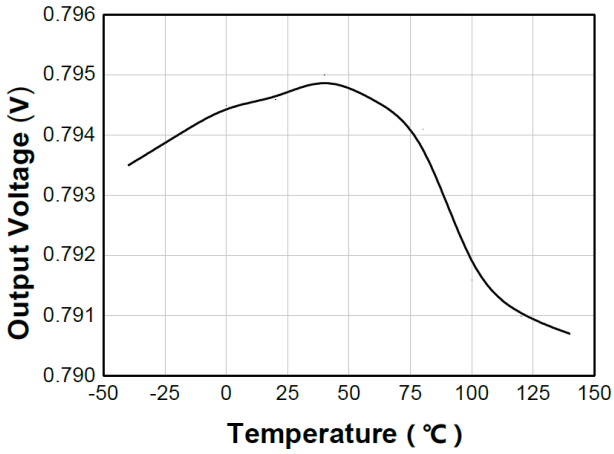


Fig.3 Enable/Disable Level vs Input Voltage

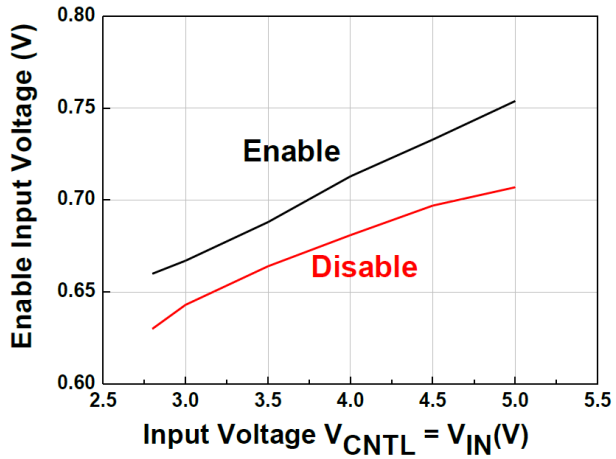


Fig.4 Line Regulation

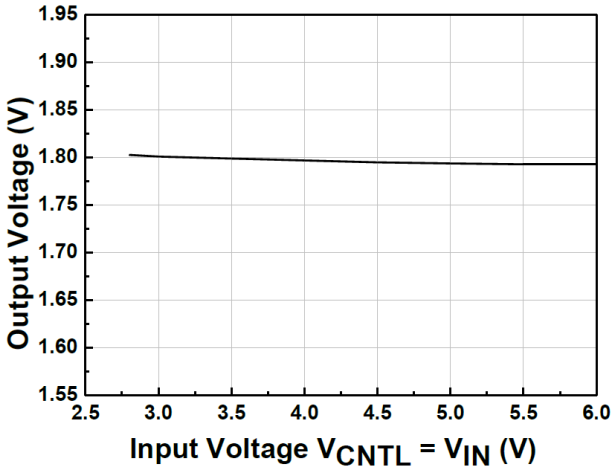


Fig.5 Quiescent Current vs Input Voltage

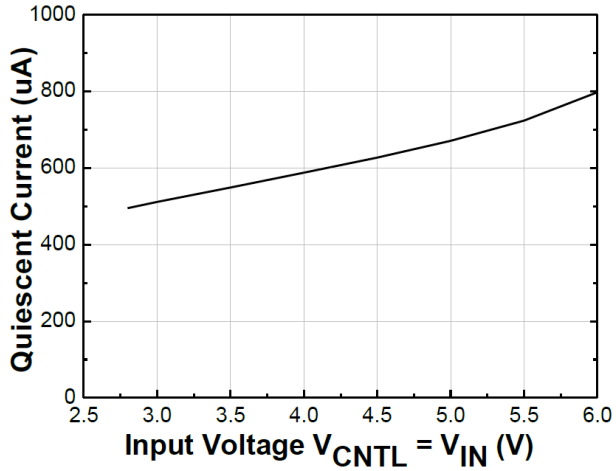


Fig.6 Quiescent Current vs Temperature

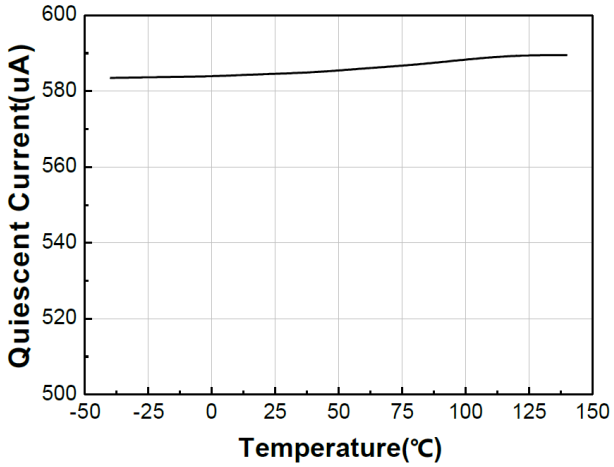


Fig.7 On Resistance vs Temperature

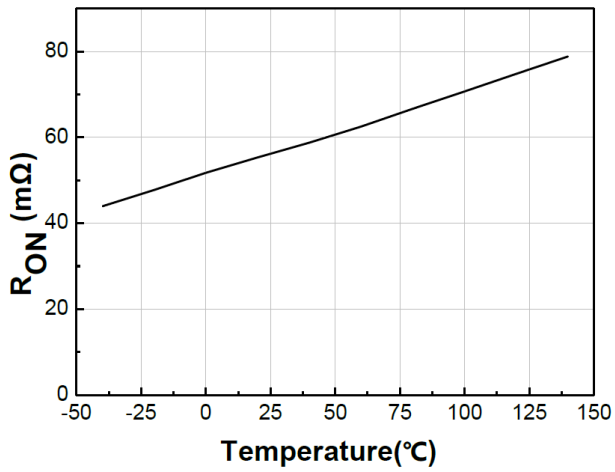


Fig.8 Output Voltage vs Temperature
(C_{IN}=C_{OUT}=10uF)

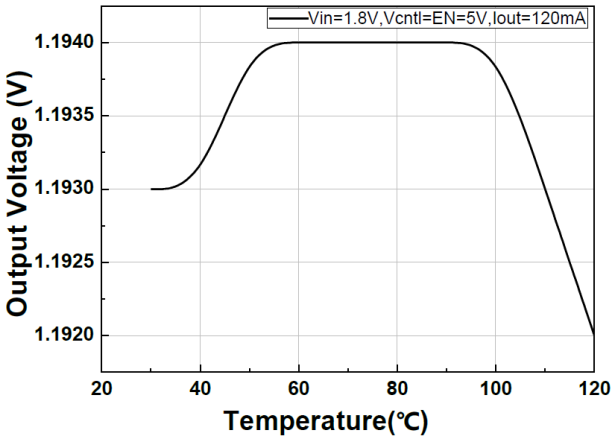
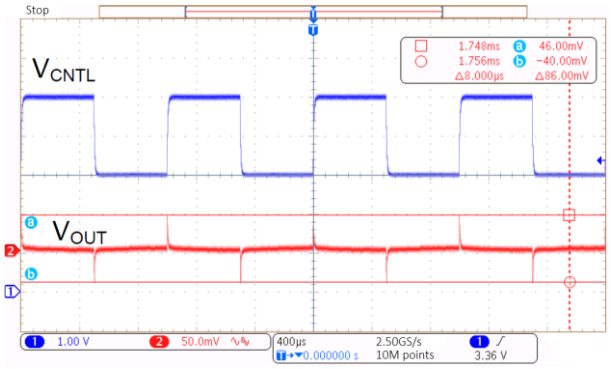


Fig.9 Input Voltage Transient Response

(V_{CNTL}=CE=3-5.0V, V_{IN}=1.8V, C_{IN}=C_{OUT}=10uF, I_{OUT}=800mA)



(V_{CNTL}=CE=5.0V,V_{IN}=1-3.0V,C_{IN}=C_{OUT}=10uF, I_{OUT}=100mA)

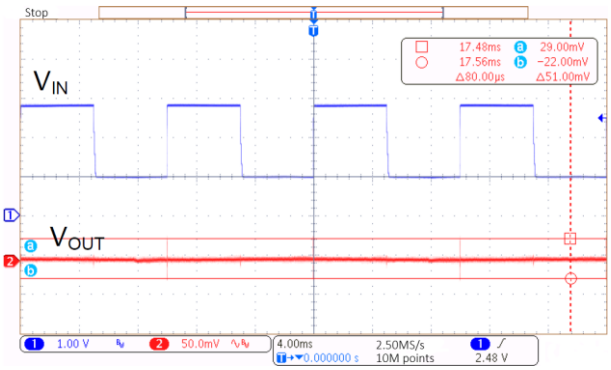
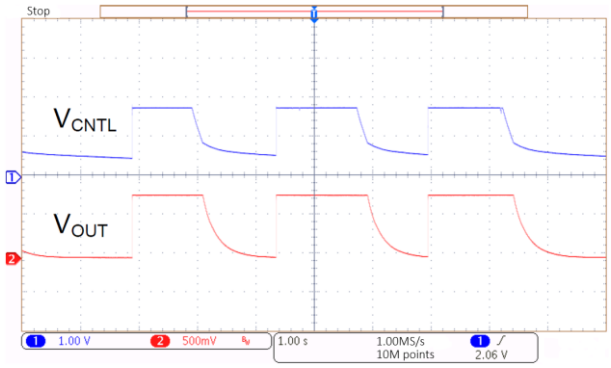


Fig.10 Over Shoot

V_{CNTL}=5.0V, V_{IN}=1.8V, C_{IN}=C_{OUT}=10uF, I_{OUT}=0A Hot-swap V_{CNTL} and V_{IN} respectively



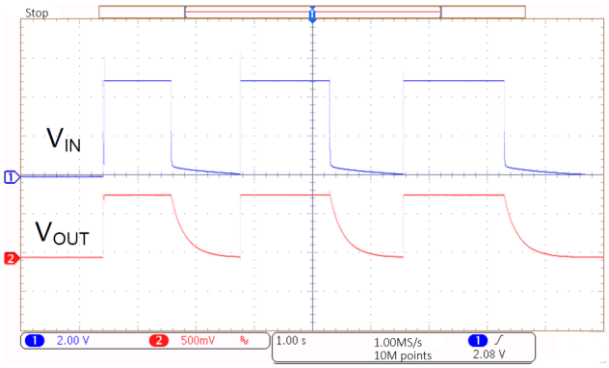


Fig.11 Load Transient Response

(V_{CNTL} =CE=5.0V, V_{IN}=1.8V C_{IN}=C_{OUT}=10uF, I_{OUT} =100mA-2A)

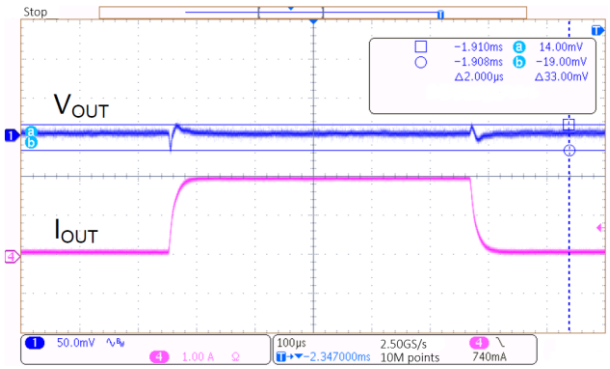


Fig.12 V_{IN} Turn ON

(V_{CNTL} =5V, V_{IN} = 3.3V, C_{OUT} = 1000uF, No Load)

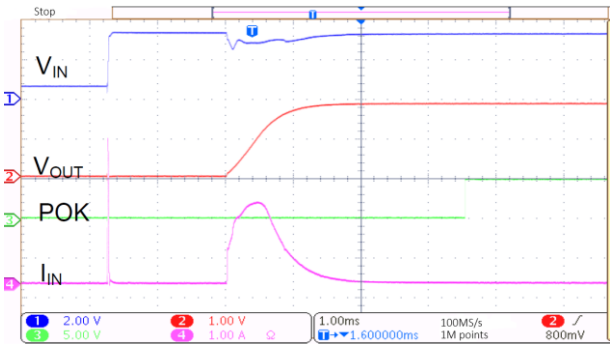
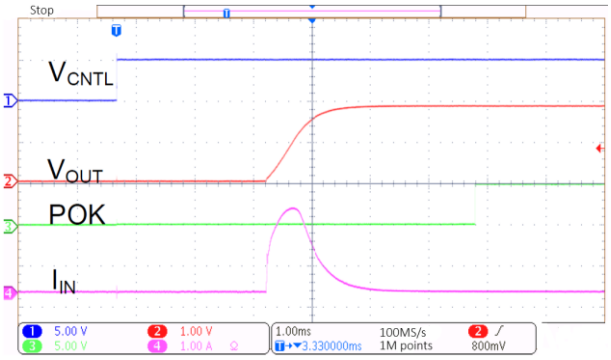
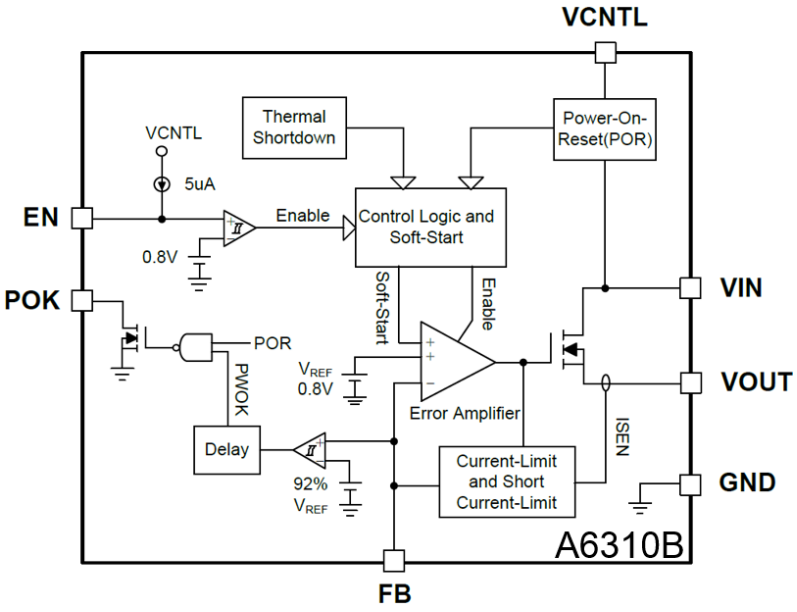


Fig.13 V_{CNTL} Turn ON

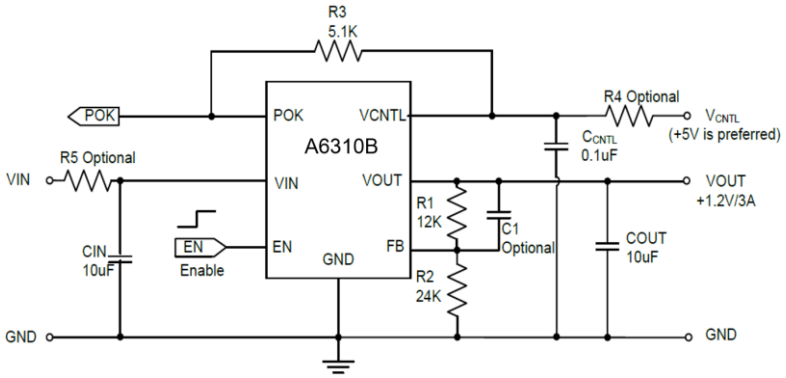
(V_{CNTL} =5V, V_{IN} = 3.3V, C_{OUT} = 1000uF, No Load)



BLOCK DIAGRAM



DETAILED INFORMATION



Setting the Output Voltage

Through FB external resistance voltage dividing, the output voltage value can be calculated according to the following formula:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

V_{OUT} can choose the voltage from 0.8V to 5.0V and the center value of VFB is 0.8V. When the output voltage is 0.8V, R1 can use 0 Ω resistance or direct short circuit.

Setting the Input Capacitor and the Output Capacitor

Input and output capacitors are recommended to use more than 10uF, which can ensure the stability of the system, and C_{OUT} must be less than 1000uF.

Setting the Feedback Capacitor -C1

It is suggested that the feedback capacitor C1 be used, which can improve the transient load desirability and system stability.

Setting the Current limiting resistors- R4, R5

R4 and R5 are current limiting resistors. It is recommended to add R4 and R5 resistors when the input voltage is high. Where R4 is usually recommended 0-2 ohms. Since R5 is a power path, R5 needs to be set according to the maximum load requirement. It is generally recommended that the ripple introduced by R5 should not exceed 0.5V.

PCB Layout

In order to get better use effect, the main points for attention of PCB layout are as follows:

1.The input and output capacitors are as close as possible to the chip pins.

2.The wiring of V_{IN} and V_{OUT} should be as thick as possible to reduce the wiring resistance and improve the load performance.

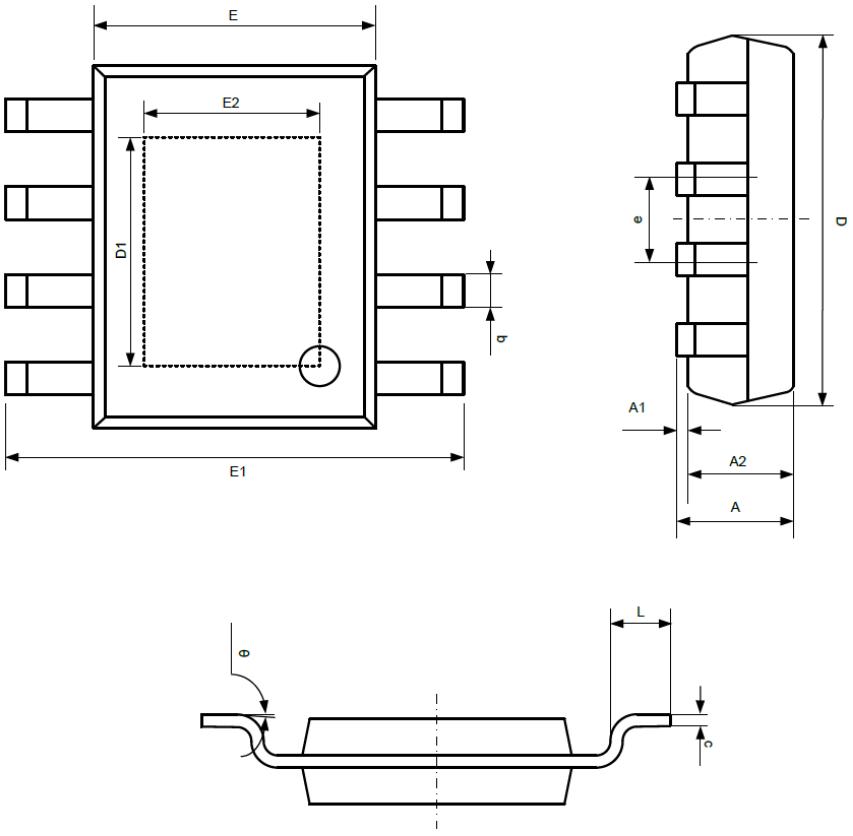
3.The route from R2 to GND uses a dedicated channel to prevent parasitic resistance from introducing into the change path, which results in incorrect feedback ratio and output error.

Input Voltage

V_{IN} and V_{CNTL} at the same potential is not recommended because this application will affect the driving of A6310B

PACKAGE INFORMATION

Dimension in PSOP8 (Unit: mm)



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.050	0.150
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.202	3.420
E	3.800	4.000
E1	5.800	6.200
E2	2.313	2.513
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

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