



DESCRIPTION

The A7240 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 4A of output current. Current mode PWM control allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. On top of the integrated internal synchronous rectifier that eliminates external Schottky diode, A7240 also employs a proprietary control scheme that switches the device into a power save mode during light load, thereby extending the range of high efficiency operation. Therefore, A7240 is a much superior solution in comparison to other competitions in terms of efficiency and cost. Overall, A7240 is a highly efficient and robust solution for DC-DC step-down applications that requires wide input ranges.

The A7240 is available in PSOP8 package.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 2,500pcs/Reel	MP8	A7240MP8R
		A7240MP8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

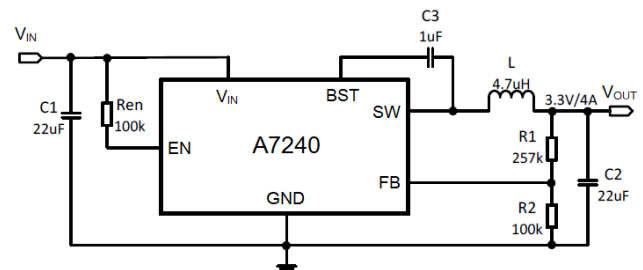
FEATURES

- Wide Input Operating Range from 4.2V to 16V
- High Efficiency: Up to 95% at Light Load
- Capable of Delivering 4A
- No external Schottky Diode Needed
- Inductor Short Circuit Protection
- Current Mode Control
- 0.923V Reference for Low Output Voltages
- Logic Control Shutdown
- Thermal Shutdown and UVLO
- Available in PSOP8 package

APPLICATION

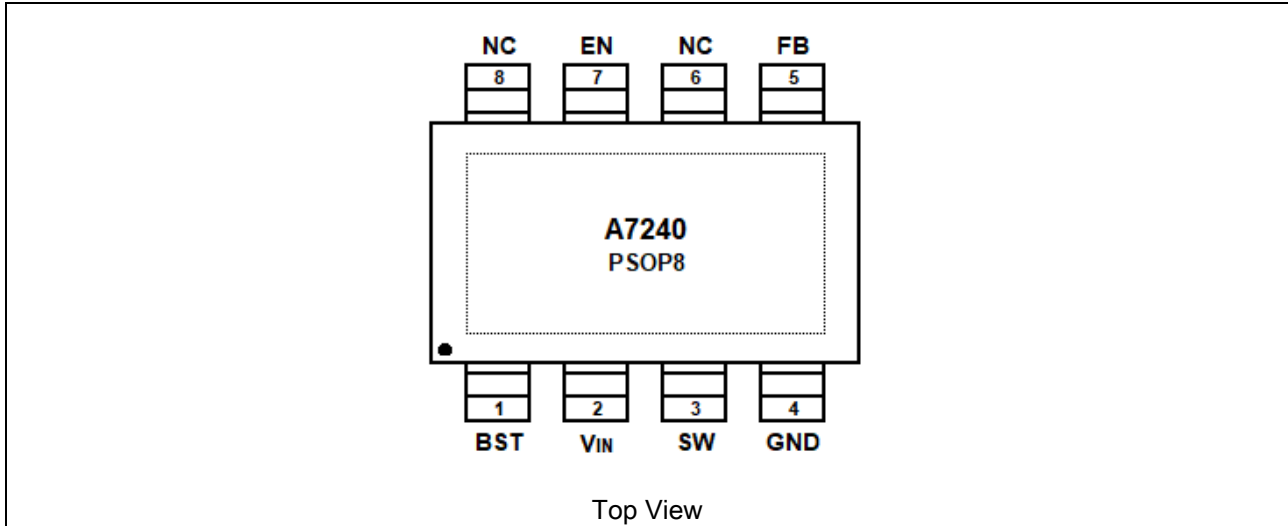
- LCD TVs
- Notebook computers
- FPGA power supplies
- LED drivers

TYPICAL APPLICATION





PIN DESCRIPTION



Pin #	Symbol	Description
1	BST	High side power transistor gate drive boost input.
2	V _{IN}	Power input. Bypass with a 10uF~22uF ceramic capacitor to GND.
3	SW	Power switching node to connect inductor.
4	GND	Ground
5	FB	Feedback input with reference voltage set to 0.923V.
6	NC	No connection
7	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
8	NC	No connection



ABSOLUTE MAXIMUM RATINGS

Input Voltage	-0.3V ~ 17V
SW.EN Voltage	-0.3V ~ $V_{IN} + 0.3V$
BST Voltage	-0.3V ~ SW +6V
FB Voltage	-0.3V ~ 6V
SW to Ground Current	Internally Limited
T _A , Ambient Temperature	-40°C ~ 85°C
T _S , Storage Temperature	-55°C ~ 150°C

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{IN}=12V$, $V_{OUT}=5V$, $T_A=25^\circ C$, unless otherwise stated

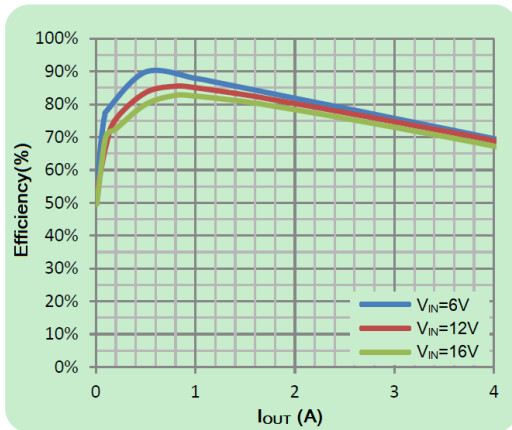
Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.2	-	16	V
UVLO Threshold		-	4.1	-	V
Supply Current in Operation	$V_{EN} = 2.0V$, $V_{FB} = 1.1V$	-	0.5	-	mA
Supply Current in Shutdown	$V_{EN} = 0V$ or $V_{EN} = GND$	-	5	10	uA
Regulated Feedback Voltage	$4.2V \leq V_{IN} \leq 16V$	0.904	0.923	0.942	V
High-side Switch On Resistance	$V_{BST-SW} = 5V$	-	120	-	mΩ
Low-side Switch On Resistance	$V_{IN} = 5V$	-	60	-	mΩ
High-side Switch Leakage Current	$V_{EN} = 0V$, $V_{SW} = 0V$	-	0	10	uA
Upper Switch Current Limit	Minimum Duty Cycle	-	6	-	A
Oscillation Frequency		-	500	-	kHz
Maximum Duty Cycle	$V_{FB} = 0.8V$	-	92	-	%
Minimum On Time		-	100	-	ns
EN Input Voltage "H"		1.5	-	-	V
EN Input Voltage "L"		-	-	0.6	V
Thermal Shutdown		-	160	-	°C



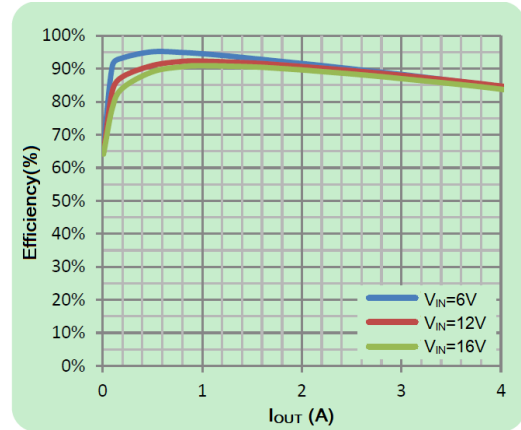
TYPICAL PERFORMANCE CHARACTERISTICS

$L=4.7\mu\text{H}$, $C_{\text{IN}}=22\mu\text{F}$, $C_{\text{OUT}}=22\mu\text{F}$, $T_A=25^\circ\text{C}$, unless otherwise stated

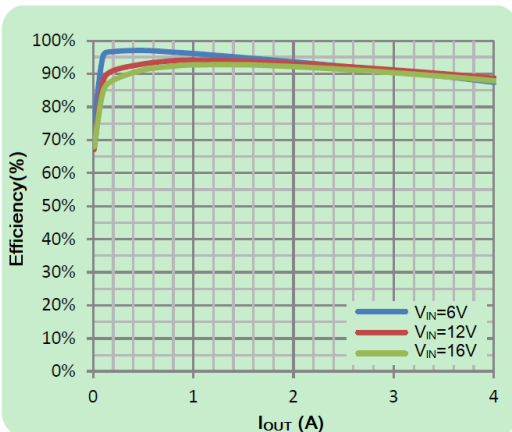
1. Efficiency vs. I_{OUT} , $V_{\text{OUT}}=1.2\text{V}$



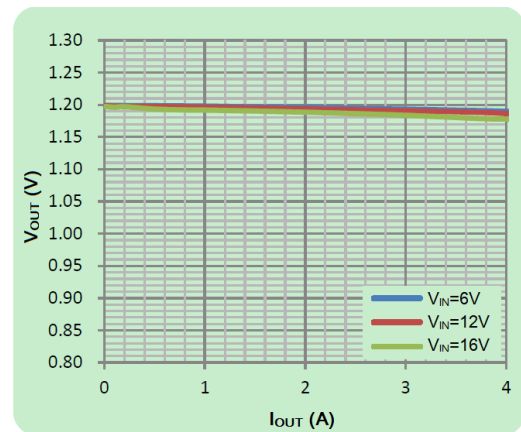
2. Efficiency vs. I_{OUT} , $V_{\text{OUT}}=3.3\text{V}$



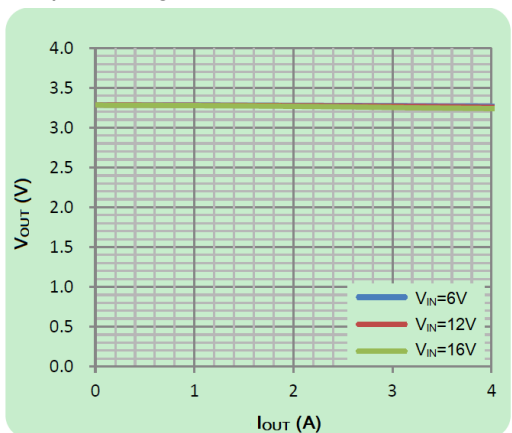
3. Efficiency vs. I_{OUT} , $V_{\text{OUT}}=5.0\text{V}$



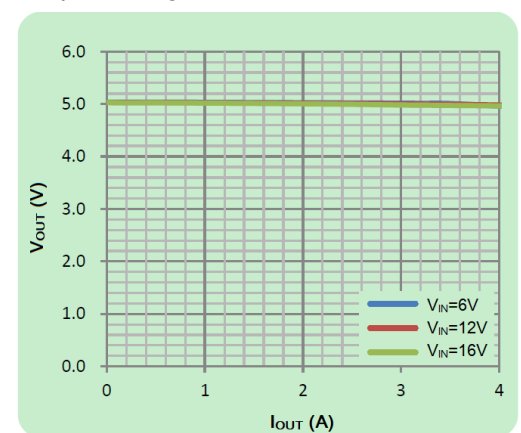
4. Output Voltage vs. I_{OUT} , $V_{\text{OUT}}=1.2\text{V}$



5. Output Voltage vs. I_{OUT} , $V_{\text{OUT}}=3.3\text{V}$

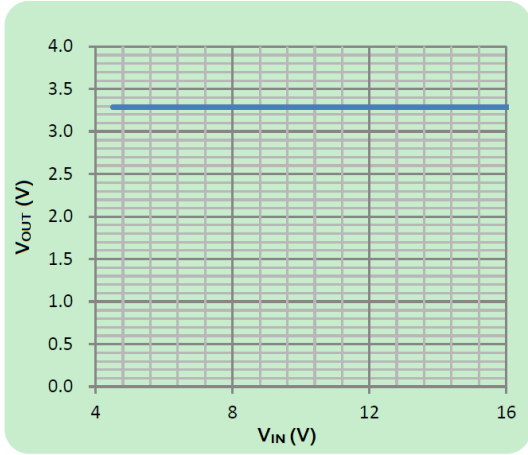


6. Output Voltage vs. I_{OUT} , $V_{\text{OUT}}=5.0\text{V}$

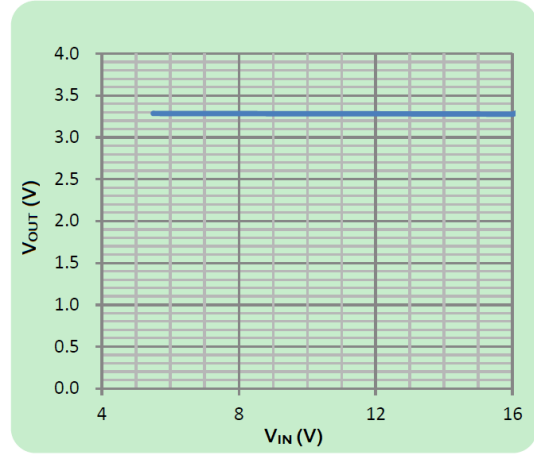




7. V_{OUT} vs. V_{IN} , $I_{OUT}=0$



8. V_{OUT} vs. V_{IN} , $I_{OUT}=1A$





DETAILED INFORMATION

FUNCTIONAL DESCRIPTIONS

Loop Operation

The A7240 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 4A of output current, integrated with a 120/60mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 6A (typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. Unlike the traditional method of current limiting by limiting the voltage at the compensation pin, which usually has large variation due to duty cycle variance, this type of peak current limiting scheme provides a relatively more accurate limit for output current, thereby lowering the requirements for system design.

Light Load Operation

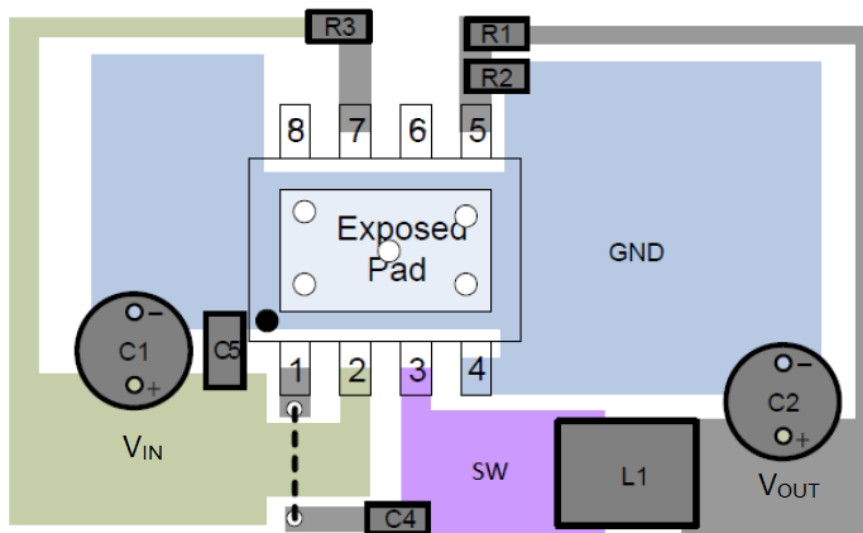
Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite RDSONs of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. A7240 employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power save mode during light load, thereby extending the range of high efficiency operation.



PCB LAYOUT RECOMMENDATION

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

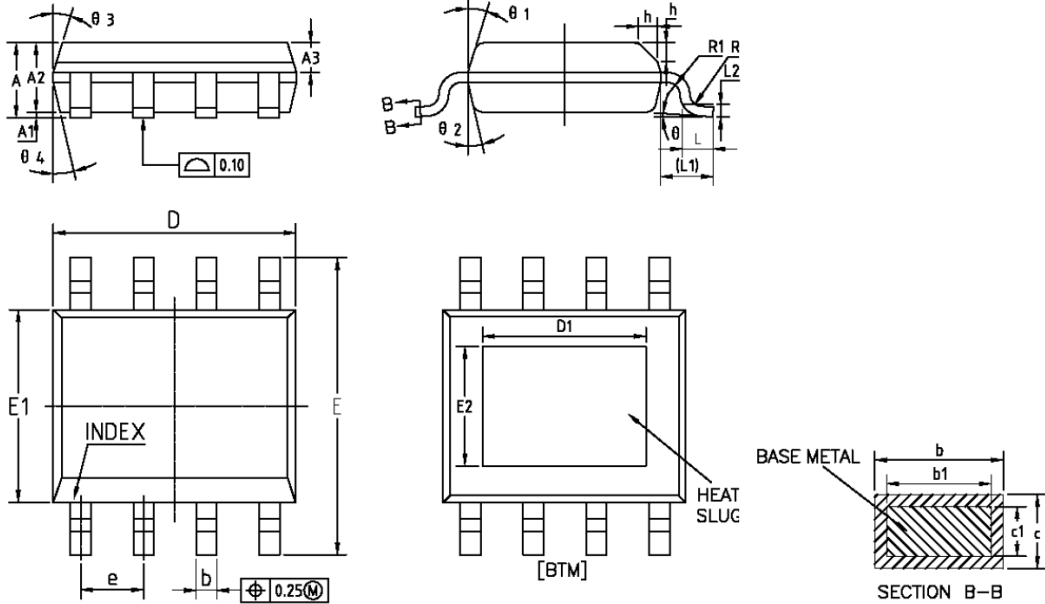
1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (SW).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.





PACKAGE INFORMATION

Dimension in PSOP8 Package (Unit: mm)



Symbol	Min	Max
A	1.35	1.75
A1	0.00	0.15
A2	1.25	1.65
A3	0.50	0.70
b	0.38	0.51
b1	0.37	0.47
c	0.17	0.25
c1	0.17	0.23
D	4.80	5.00
D1	3.10	3.50
E	5.80	6.20
E1	3.80	4.00
E2	2.20	2.60
e	1.27 BSC	
L	0.45	0.80
L1	1.04 REF	
L2	0.25 BSC	
R	0.07	-
R1	0.07	-
h	0.30	0.50
θ	0°	8°
θ1	15°	19°
θ2	11°	15°
θ3	15°	19°
θ4	11°	15°



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